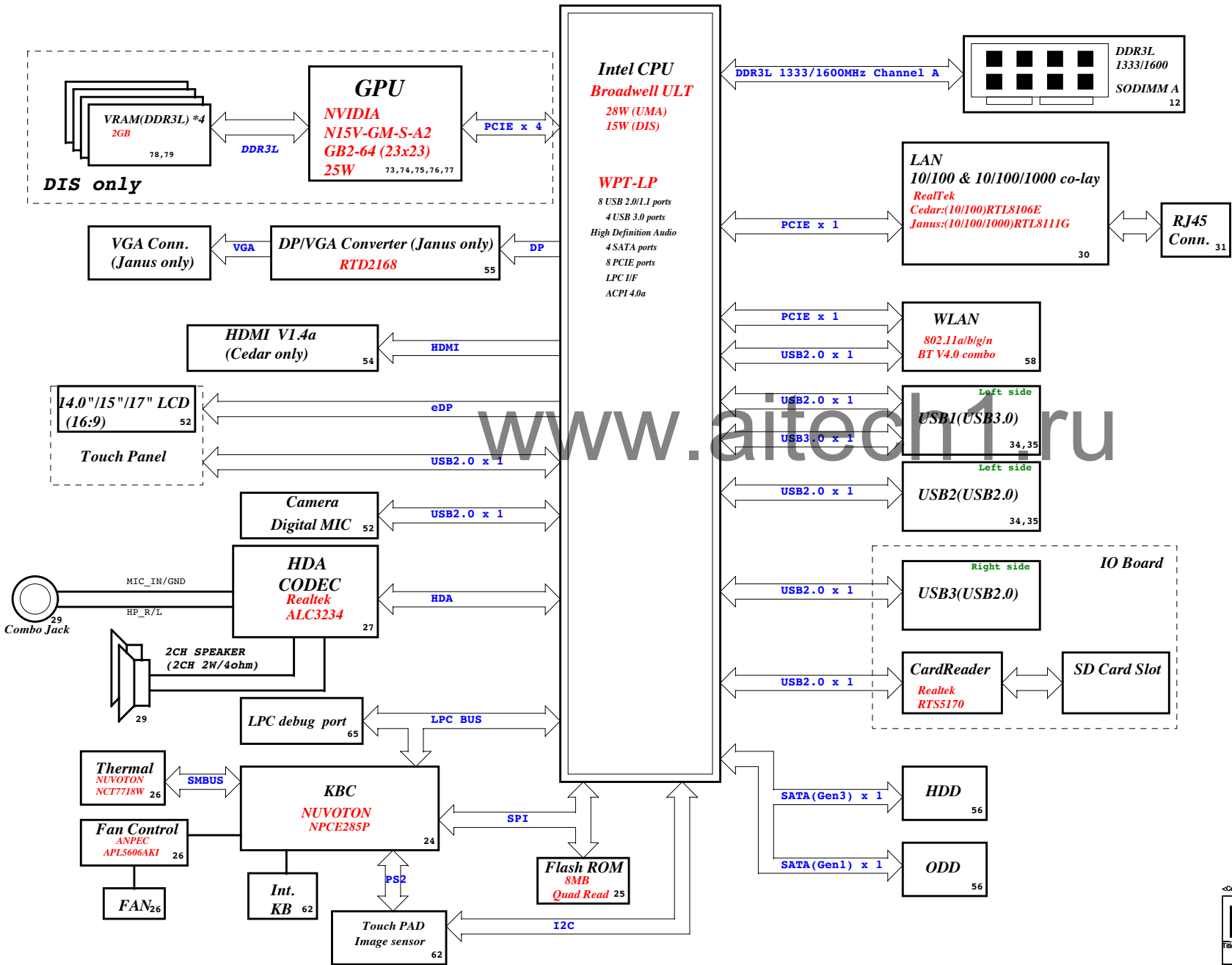


Project code:4PD00I010001
PCB P/N: 13269-1
Revision: X02

Cedar/Janus Block Diagram



CHARGER	
HPA02224RGRR-1-GP 44	
INPUTS	OUTPUTS
AD+	DCBATOUT
BT+	
SYSTEM DC/DC	
TPS51225RUKR-GP 45	
INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 5V_AUX_S5 5V_S5 3D3V_S5
CPU Core Power	
ISL95813HR2-GP 46,47	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
DDR3L SUS	
TPS51716RUKR-GP 49	
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3 0D65V_S0
CPU 1.05V	
RT8237CZQW-2-GP 48	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0
CPU 1D5V_S0	
TLV70215DBVR-GP 51	
INPUTS	OUTPUTS
3D3V_S5	1D5V_S0
Switches	
36 83	
INPUTS	OUTPUTS
1D35V_S3	1D35V_S0
5V_S5	5V_S0
3D3V_S5	3D3V_S0
1D05V_S0	1D05V_VGA_S0
3D3V_S0	3D3V_VGA_S0
1D35V_S3	1D35V_VGA_S0
PCB LAYER	
L1:Top L2:VCC L3:Signal L4:Signal L5:GND L6:Signal	

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Title

(Reserved)

Size
A4

Document Number

Janus HSW 40/50/70

Rev
A00

Date: Friday, February 07, 2014

Sheet 3 of 104

SSID = CPU

Layout Note:

Impedance control: 50 ohm

[24,42,44,46] H_PROCHOT# <<>>

[36] H_THERMTRIP_EN <<<

Layout Note: Close to CPU

[12] DDR_PG_CTRL <<<

Layout Note:

Design Guideline:

SM_RCOMP keep routing length less than 500 mils.

71.HASWE.G0U

Layout Note:

Place close to DIMM

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Title

CPU (THERMAL/MISC/PM)

Size
A4

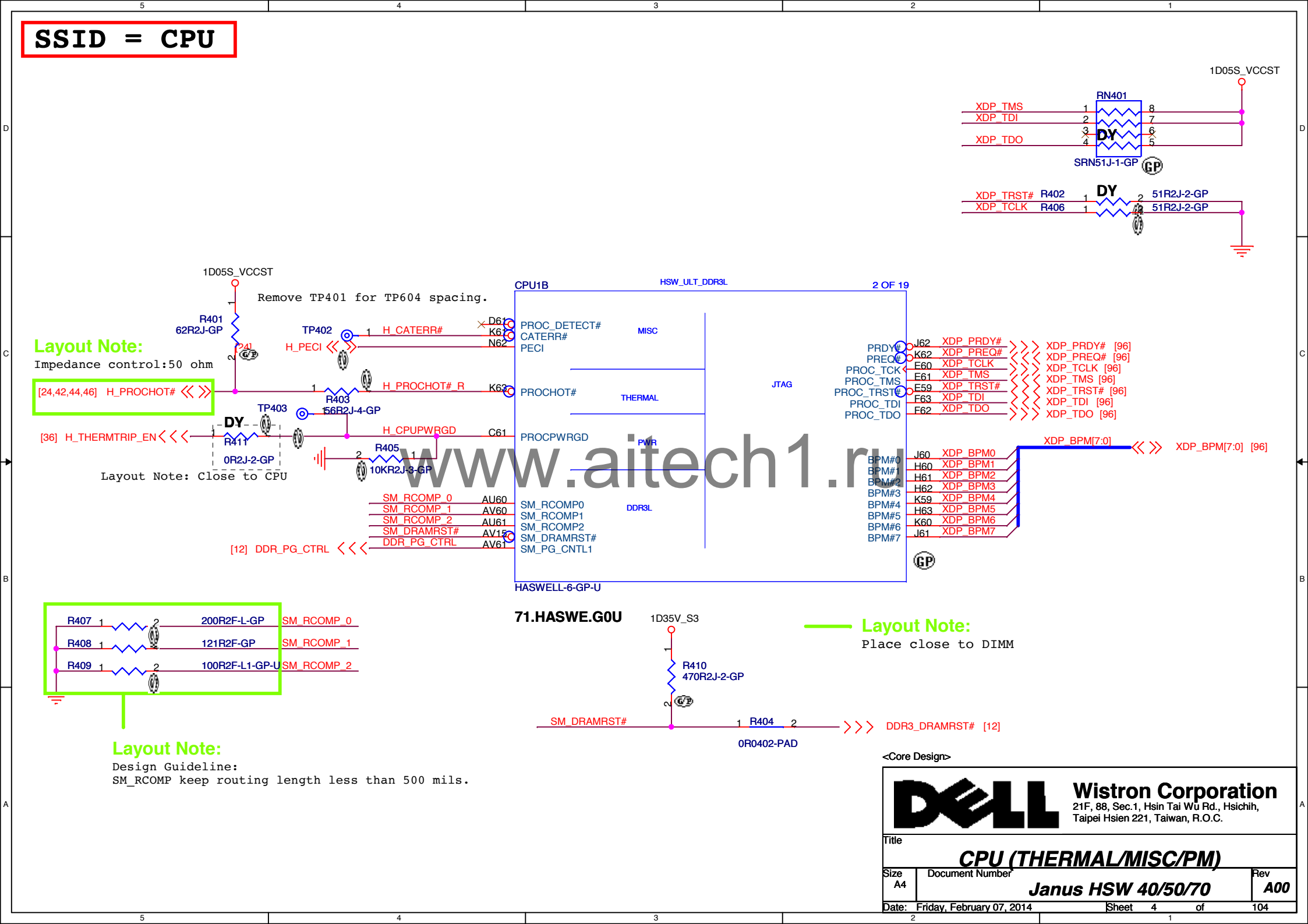
Document Number

Janus HSW 40/50/70

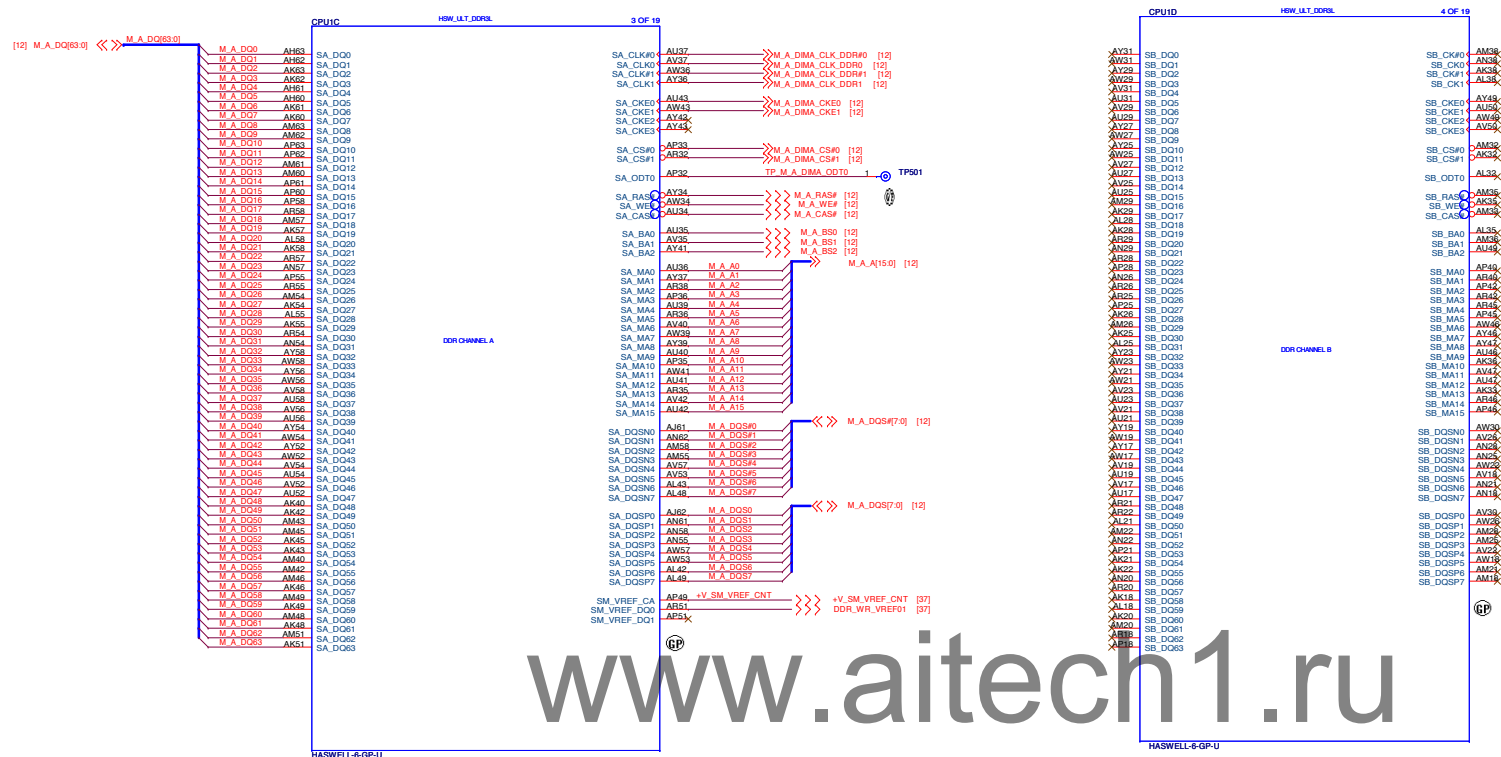
Rev
A00

Date: Friday, February 07, 2014

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DDR3L ball type: Non-Interleaved Type



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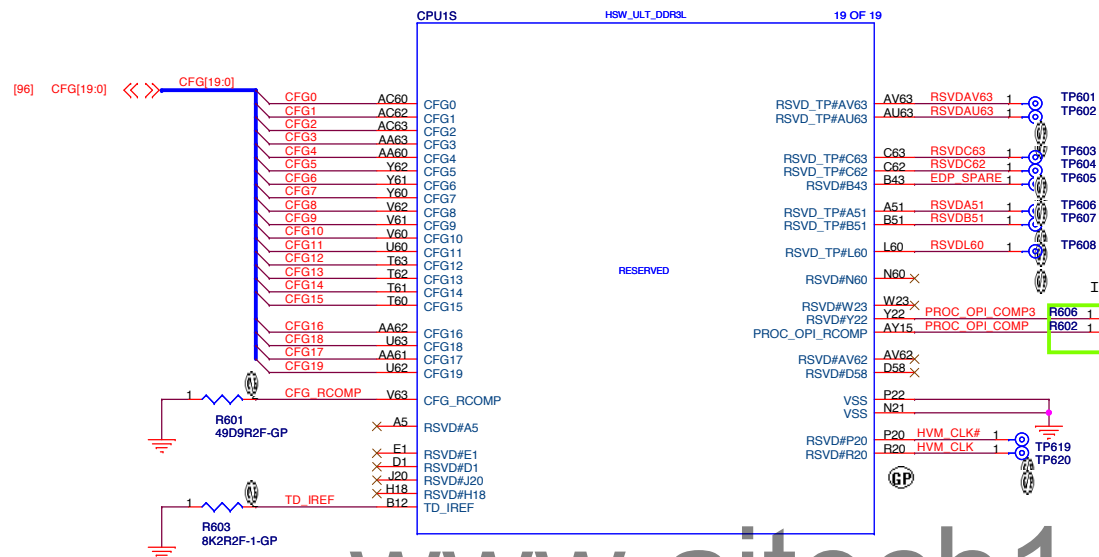
<Core Design>



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CPU (DDR)			
Size	Document Number	Rev	A00
Date	Friday, February 07, 2014	Sheet	6 of 104

SSID = CPU



#514405

7.4

Reserved or Unused Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

- RSVD - these signals should not be connected
- RSVD_TP - these signals should be routed to a test point
- RSVD_NCTF - these signals are non-critical to function and may be left unconnected

Intel Recommend

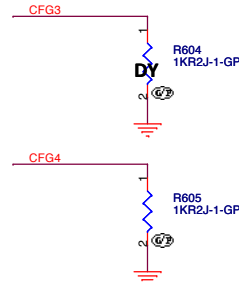
Layout Note:

1. Referenced "continuous" VSS plane only.
2. Avoid routing next to clock pins or noisy signals.
3. Trace width: 12~15mil
4. Isolation Spacing: 12mil
5. Max length: 500mil

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#514405 PCH strap pin:

Signal Name	Description	Direction / Buffer Type
CFG[19:0]	<p>Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate Platform Design Guide for pull-down recommendations when a logic low is desired.</p> <ul style="list-style-type: none">• CFG[2:0]: Reserved configuration lane. A test point may be placed on the board for these lanes.• CFG[3]: MSR Privacy Bit Feature<ul style="list-style-type: none">— 1 = Debug capability is determined by IA32_Debug_Interface_MSR (C80h) bit[0] setting— 0 = IA32_Debug_Interface_MSR (C80h) bit[0] default setting overridden• CFG[4]: eDP enable<ul style="list-style-type: none">— 1 = Disabled— 0 = Enabled• CFG[19:5]: Reserved configuration lanes. A test point may be placed on the board for these lanes.	I/O GTL



PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)

CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR 1 : DISABLED
--------	---

DISPLAY PORT PRESENCE STRAP

CFG[4]	0 : ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT 1 : DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT
--------	--

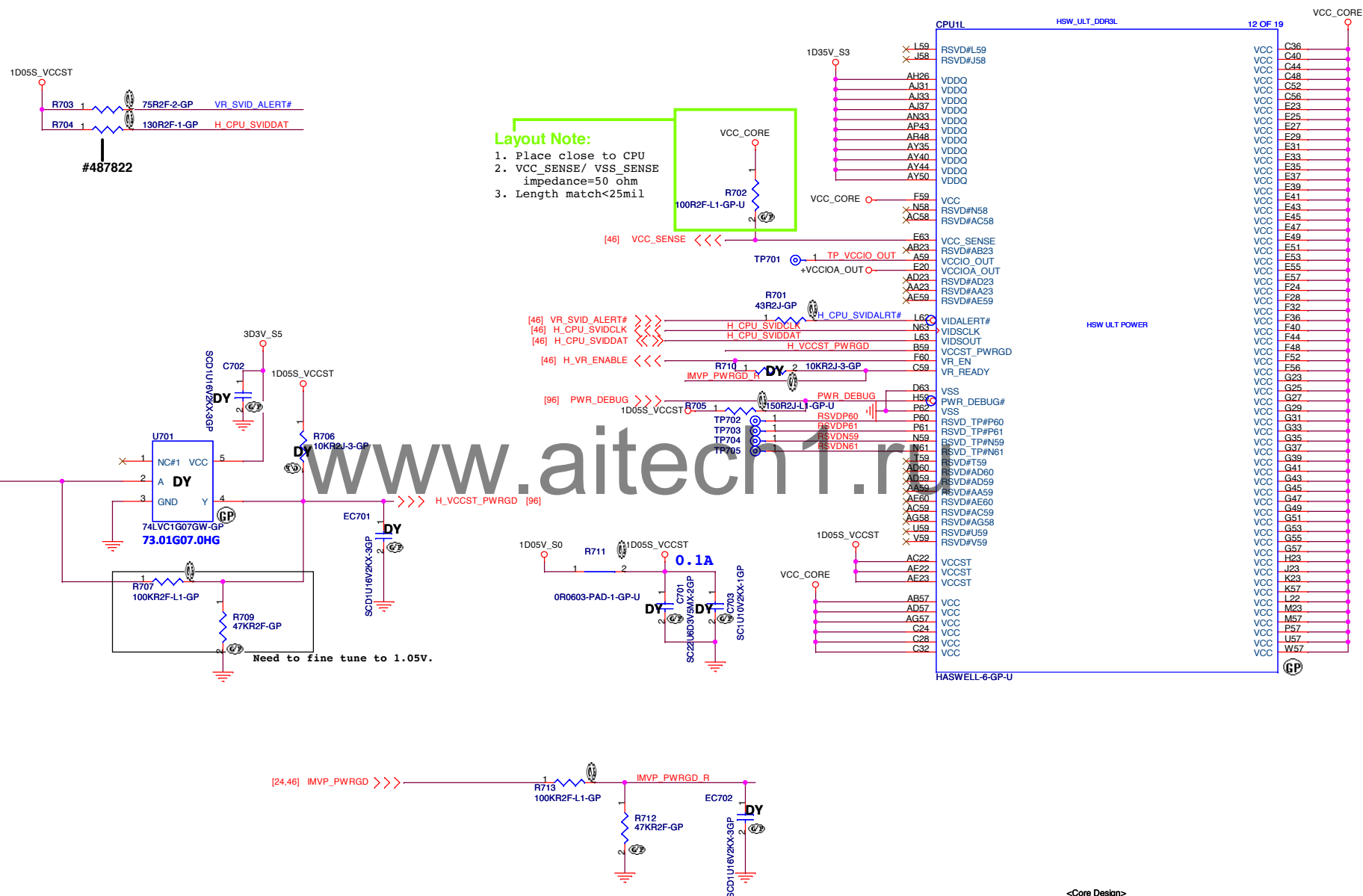
<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title		
CPU (CFG)		
Size	Document Number	Rev
A3	Janus HSW 40/50/70	A00
Date:	Friday, February 07, 2014	Sheet 6 of 104

SSID = CPU



<Core Design>



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Title

CPU (VCC CORE)Size
A3

Document Number

Janus HSW 40/50/70

Rev
A00

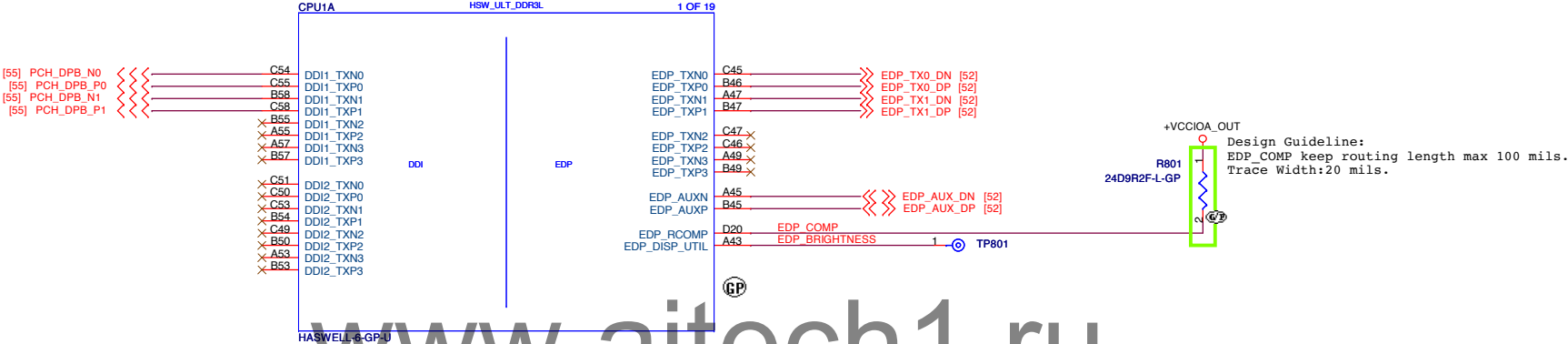
Date: Friday, February 07, 2014

Sheet 7 of 104

SSID = CPU

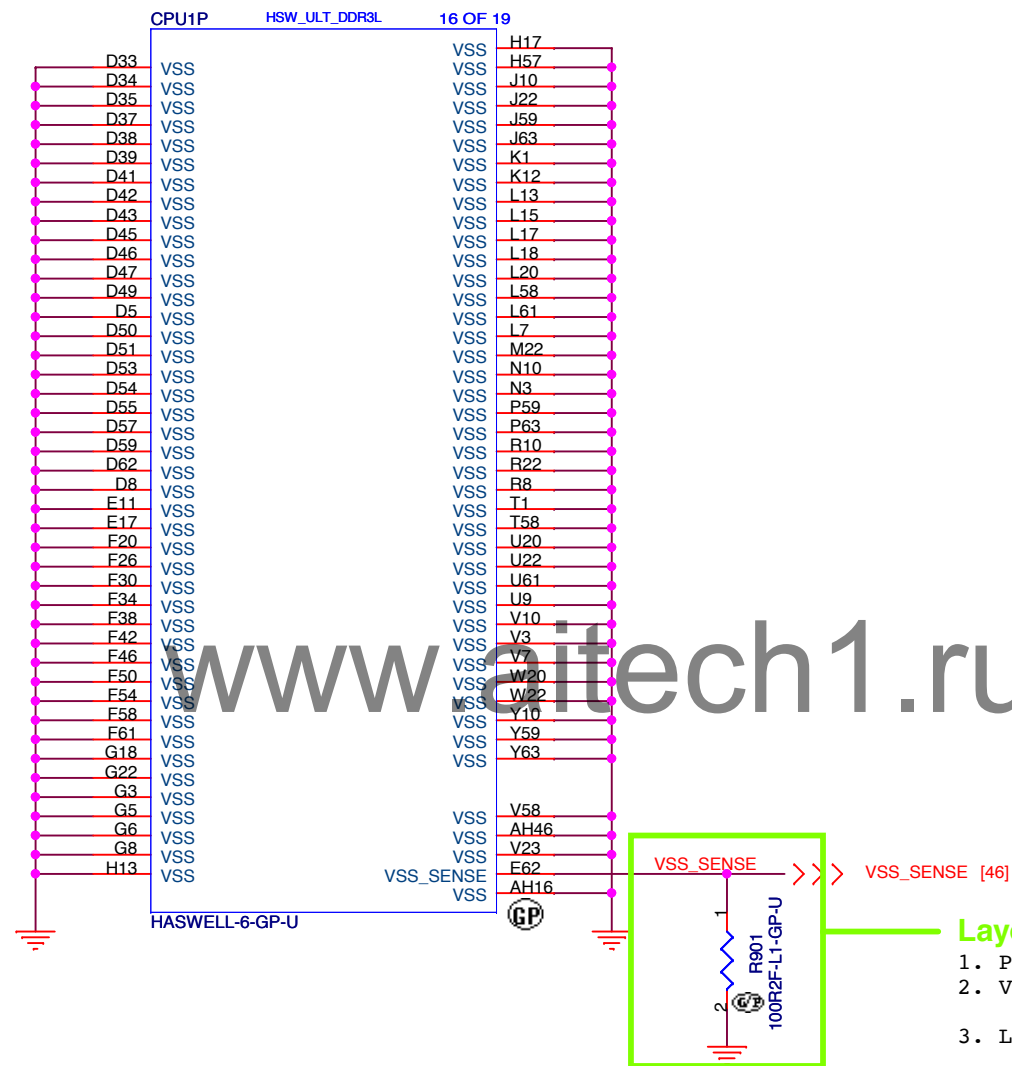
www.vinafix.vn

DP to VGA Converter



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SSID = CPU



Layout Note:

1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil

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Title

CPU (VSS)

Size
A4

Document Number

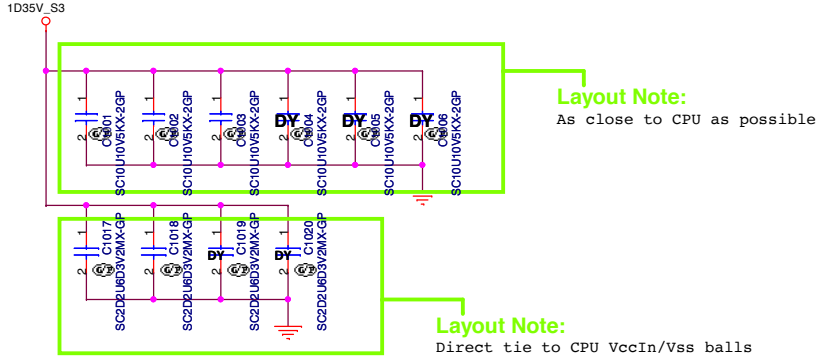
Janus HSW 40/50/70

Rev
A00

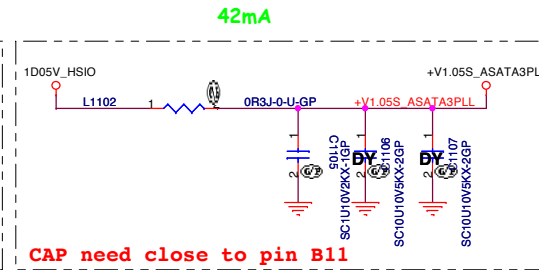
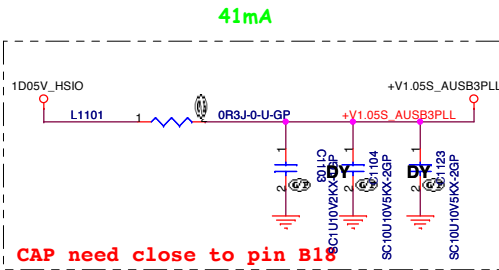
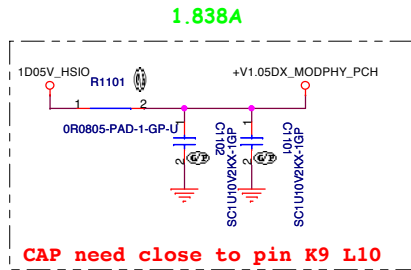
Date: Friday, February 07, 2014

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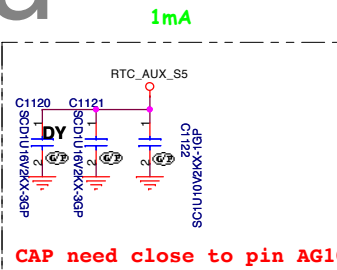
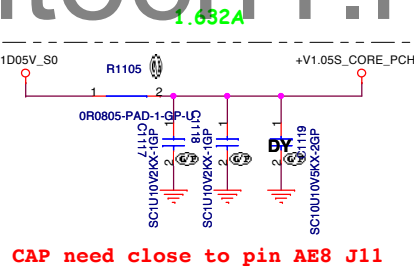
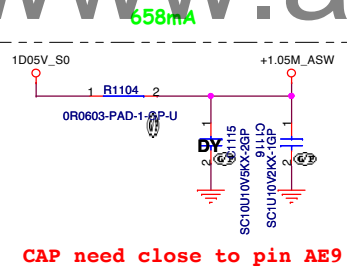
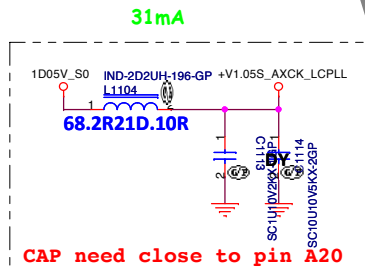
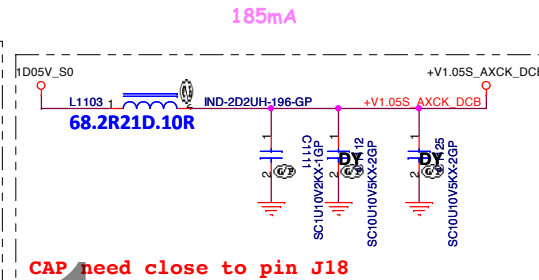
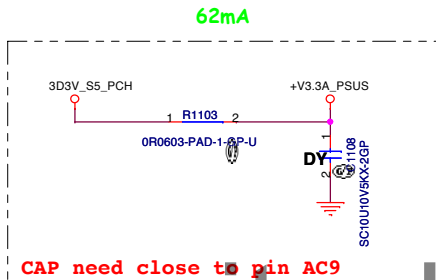
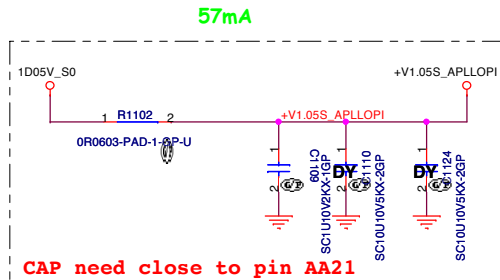
SSID = CPU



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MAX: 1.92A

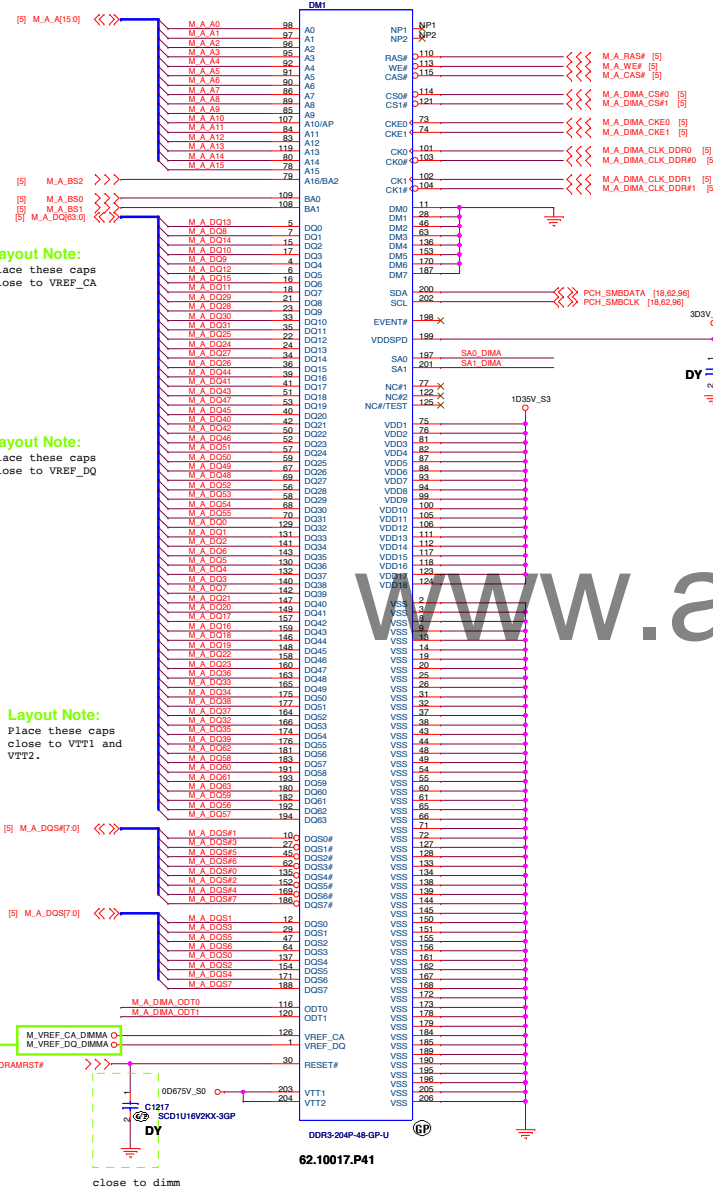


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<Core Design>

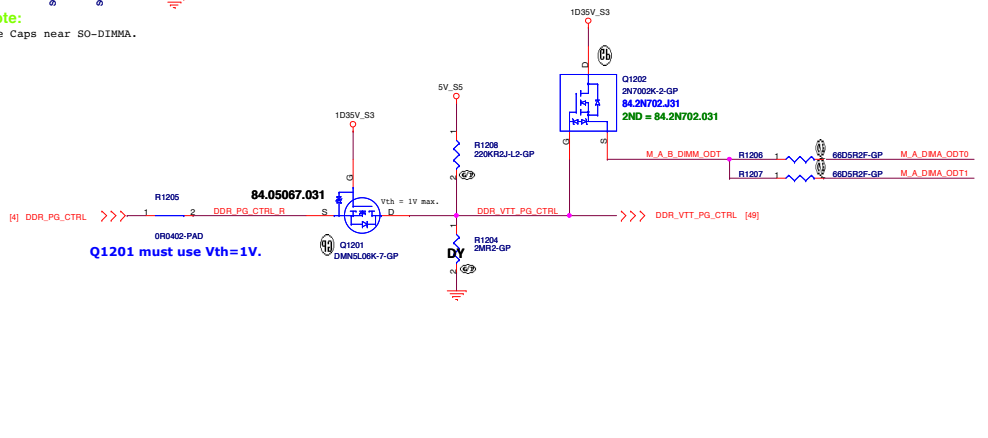
		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: CPU (Power CAP2)		
Size: A3	Document Number: Janus HSW 40/50/70	Rev: A00
Date: Friday, February 07, 2014	Sheet: 11	of 104

SSID = MEMORY



Note:
SA0 DIM0 = 0, SA1 DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30


Layout Note:
Place these Caps near SO-DIMMA.



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		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)DDR3-SODIMM2			
Size A3	Document Number Janus HSW 40/50/70		Rev A00
Date: Friday, February 07, 2014	Sheet	13	of 104

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<Core Design>

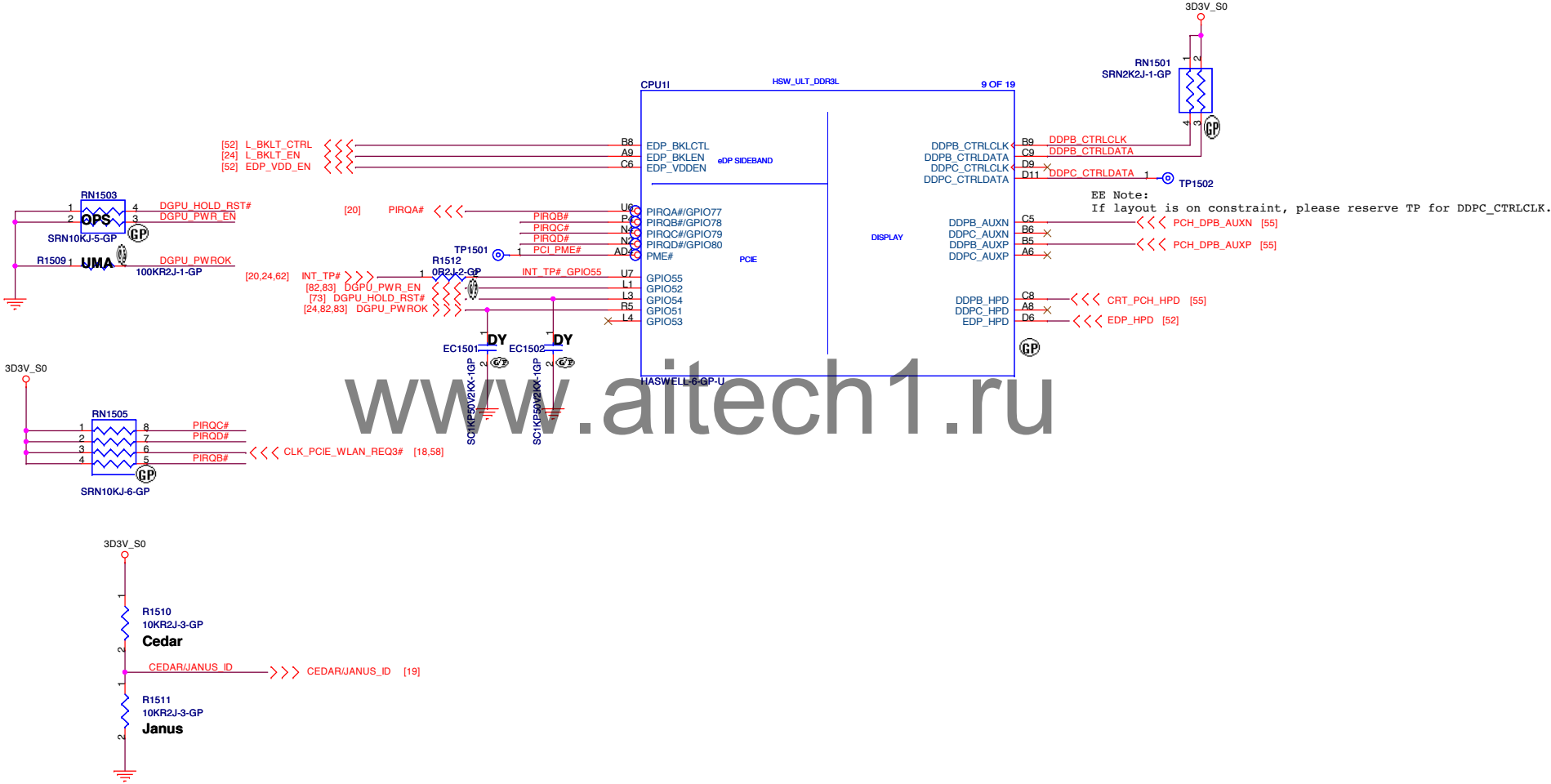
			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title (Reserved)_SODIMM _SODIMM4					
Size A4		Document Number Janus HSW 40/50/70			Rev A00
Date: Friday, February 07, 2014		Sheet 14		of 104	

SSID = CPU

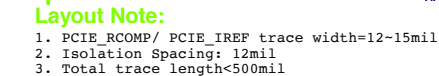
PCH strap pin:

Port B Detected	
DDPB_CTRLDATA	Low = Disable Port B (default) ★ High = Enable Port B
DDPC_CTRLDATA	★ Low = Disable Port C (default) High = Enable Port C

The internal pull-down is disabled after PLTRST# deasserts



SSID = PCH



PCIE Table

Port	Device	Share BUS
1	N/A	USB3.0_3
2	N/A	USB3.0_4
3	WLAN	
4	LAN	
5(L0-L3)	GPU	
6(L3)	HDD	SATA0
6(L2)	ODD	SATA1
6(L0-L1)	N/A	

#515621

Table 1-3. Broadwell U PCH-LP SKUs—Flexible I/O Map

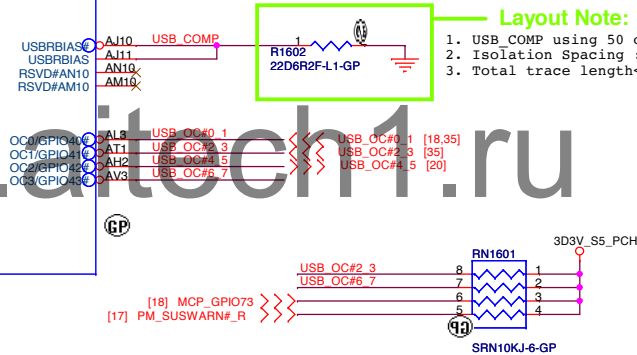
SKU	High Speed I/O Ports													
	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7	Port 8	Port 9	Port 10	Port 11	Port 12	Port 13	Port 14
Premium	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 3	USB 3.0 Port 4	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5 Lane 0 SSD	PCIe* Port 5 Lane 1 SSD	PCIe* Port 5 Lane 2	PCIe* Port 5 Lane 3	SATA 6Gb/s Port 3	SATA 6Gb/s Port 2	SATA 6Gb/s Port 1	SATA 6Gb/s Port 0
			PCIe* Port 1 SSD	PCIe* Port 2 SSD			GPU	GPU	GPU	GPU	PCIe* Port 6 Lane 0 SSD	PCIe* Port 6 Lane 1 SSD	PCIe* Port 6 Lane 2	PCIe* Port 6 Lane 3
Base	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 3	USB 3.0 Port 4	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5 Lane 0 SSD	PCIe* Port 5 Lane 1 SSD	PCIe* Port 5 Lane 2	PCIe* Port 5 Lane 3	PCIe* Port 6 Lane 0 SSD	PCIe* Port 6 Lane 1 SSD	SATA 6Gb/s Port 1	SATA 6Gb/s Port 0
			PCIe* Port 1 SSD	PCIe* Port 2 SSD			GPU	GPU	GPU	GPU				

USB 2.0 Table

Pair	Device
0	USB3.0 port1
1	USB2.0 Port2 (Debug Port)
2	USB2.0 Port3 (IOBD)
3	X
4	CAMERA
5	WLAN
6	Touch Panel
7	Card Reader

- **Layout Note:**

1. USB_COMP using 50 ohm single-ended impedance
2. Isolation Spacing :15mil
3. Total trace length<500mil



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Title

PCH (PCIE/USB)

Size
A

Document Number

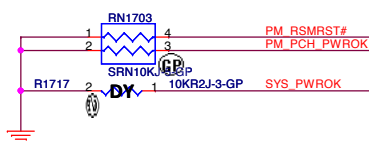
Janus HSW 40/50/70

Rev
A00

Date: Friday, February 07, 2014

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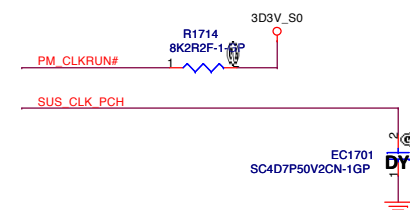
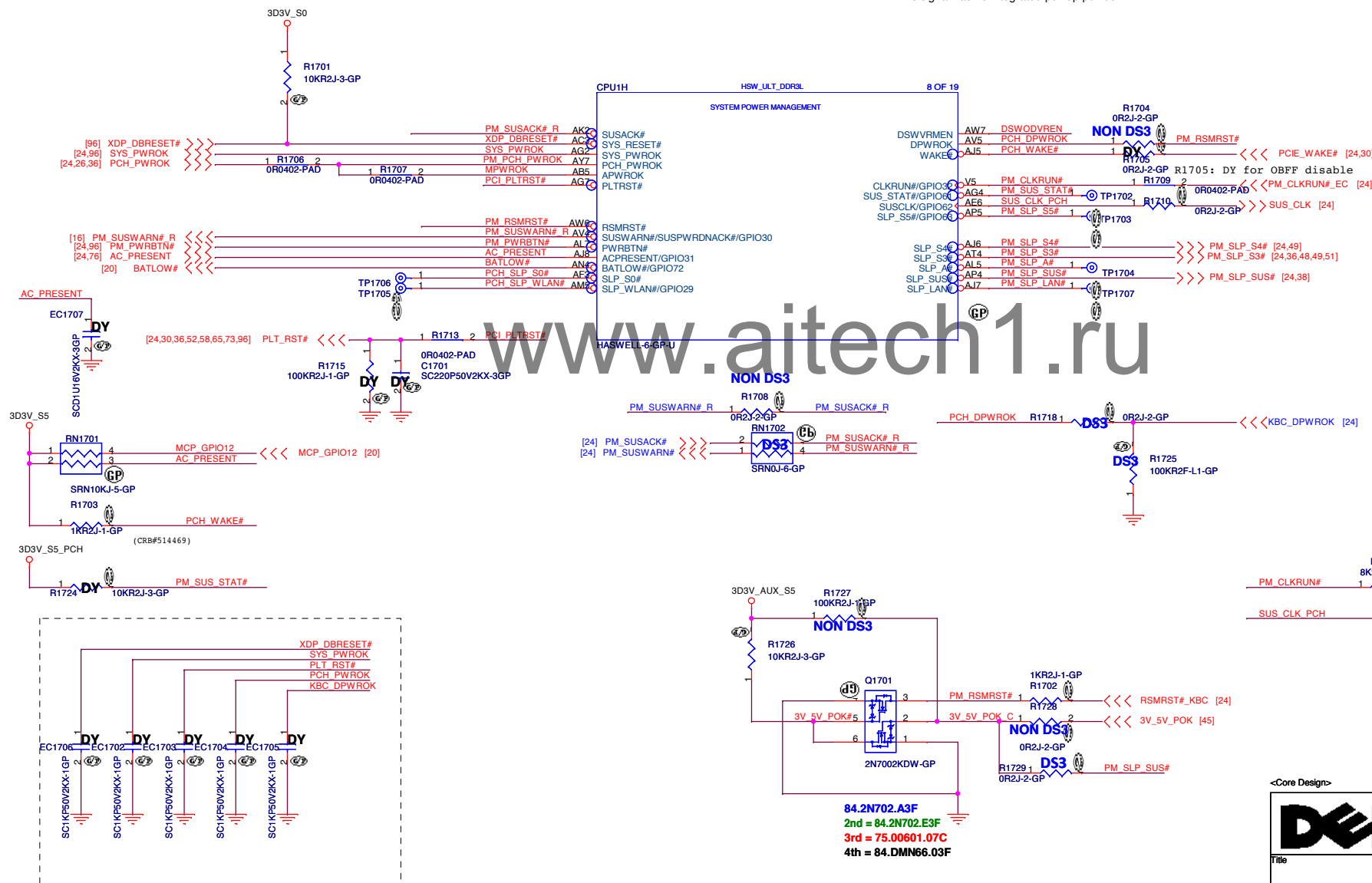
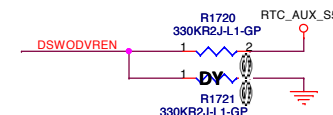
SSID = PCH



PCH strap pin:

On Die DSW VR Enable	
DSWVRMEN	Low = Disable * High = Enable (default)

This signal has no integrated pull-up/pull-down.



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Title

PCH (PM)

Size
A

Document Number

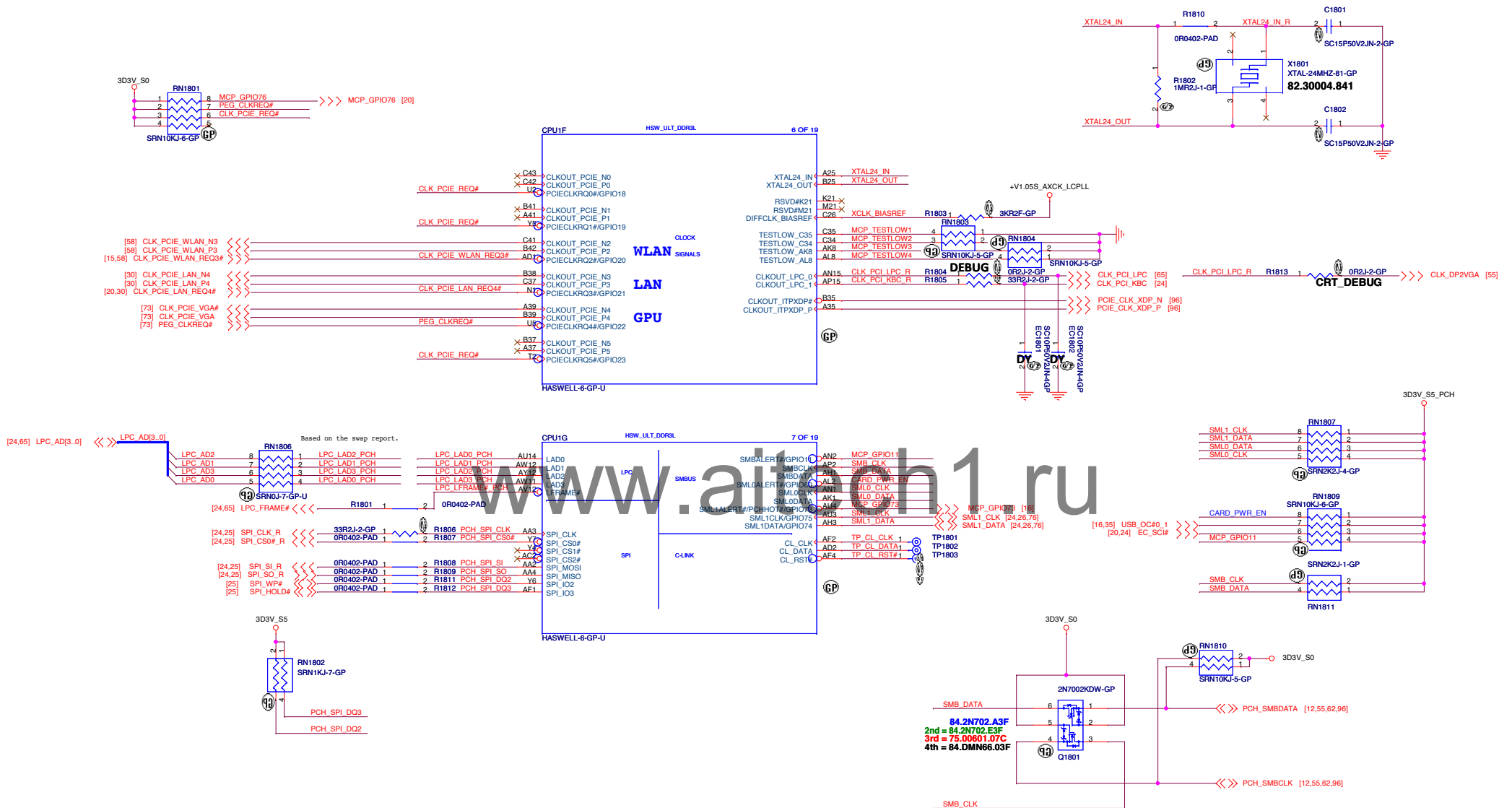
Janus HSW 40/50/70

Rev	400
-----	-----

Date: Friday, February 07, 2014

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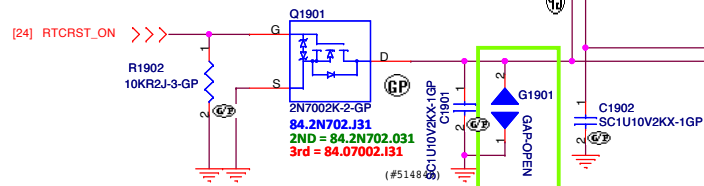
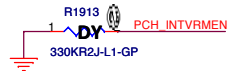
SSID = PCH



SSID = CPU

PCH strap pin:

Integrated SUS 1V VRM Enable	
INTVRMEN	Low = External VRs High = Internal VRs*

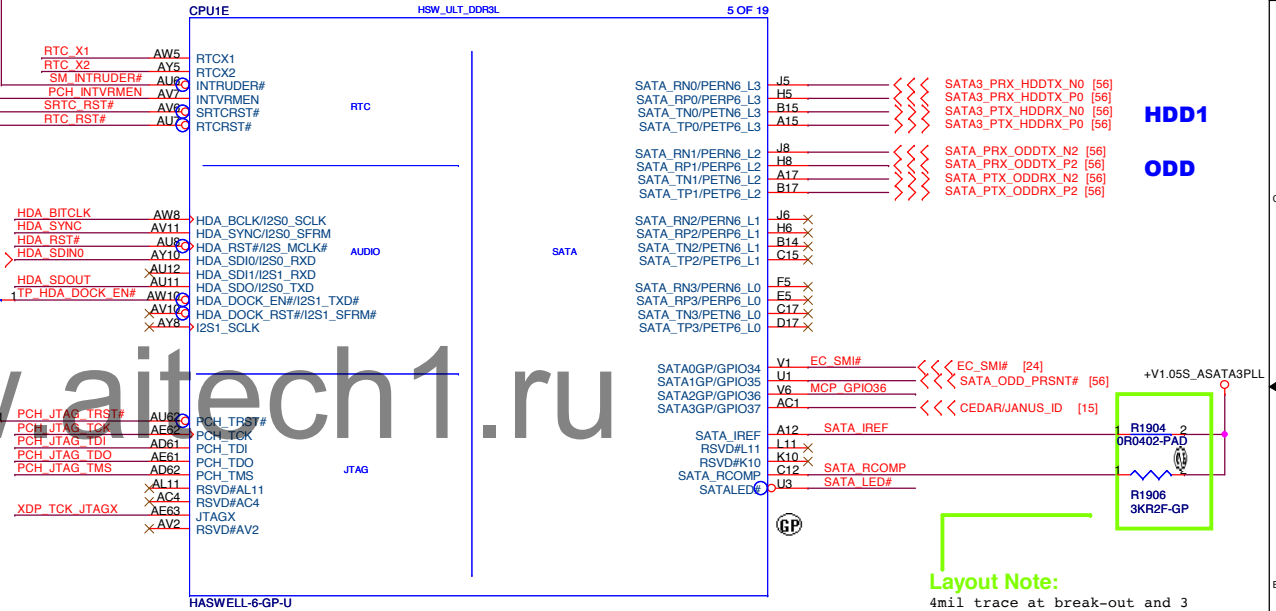
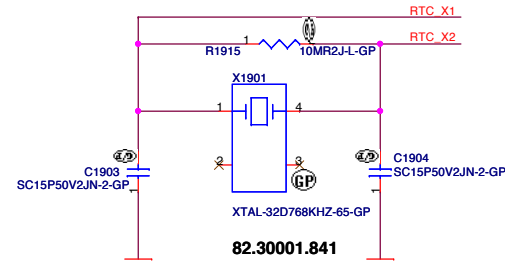
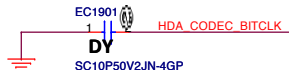
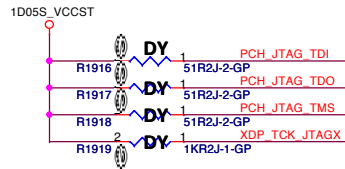
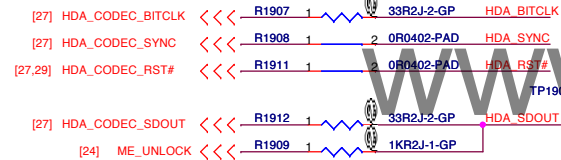


Layout: Place at the open door area.

PCH strap pin:

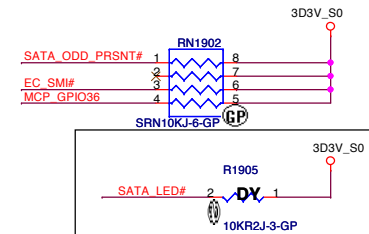
Flash Descriptor Security Override/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default * High = Enable

The internal pull-down is disabled after PLTRST# deasserts



Layout Note:

4mil trace at break-out and 3
12-15mil trace with <0.2 ohms
and length total ≤ 500 mils.



Unused SATA[3:0]GP pins must be terminated to either 3.3V rail or GND using 8.2K to 10K on the motherboard. Either pull-up or pull-down is acceptable.

<Core Design>



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Title	Author	Year	Journal	Volume	Page
...

PCH (RTC/SATA/HDA/JTAG)

Size
A3

Document Number

Janus HSW 40/50/70

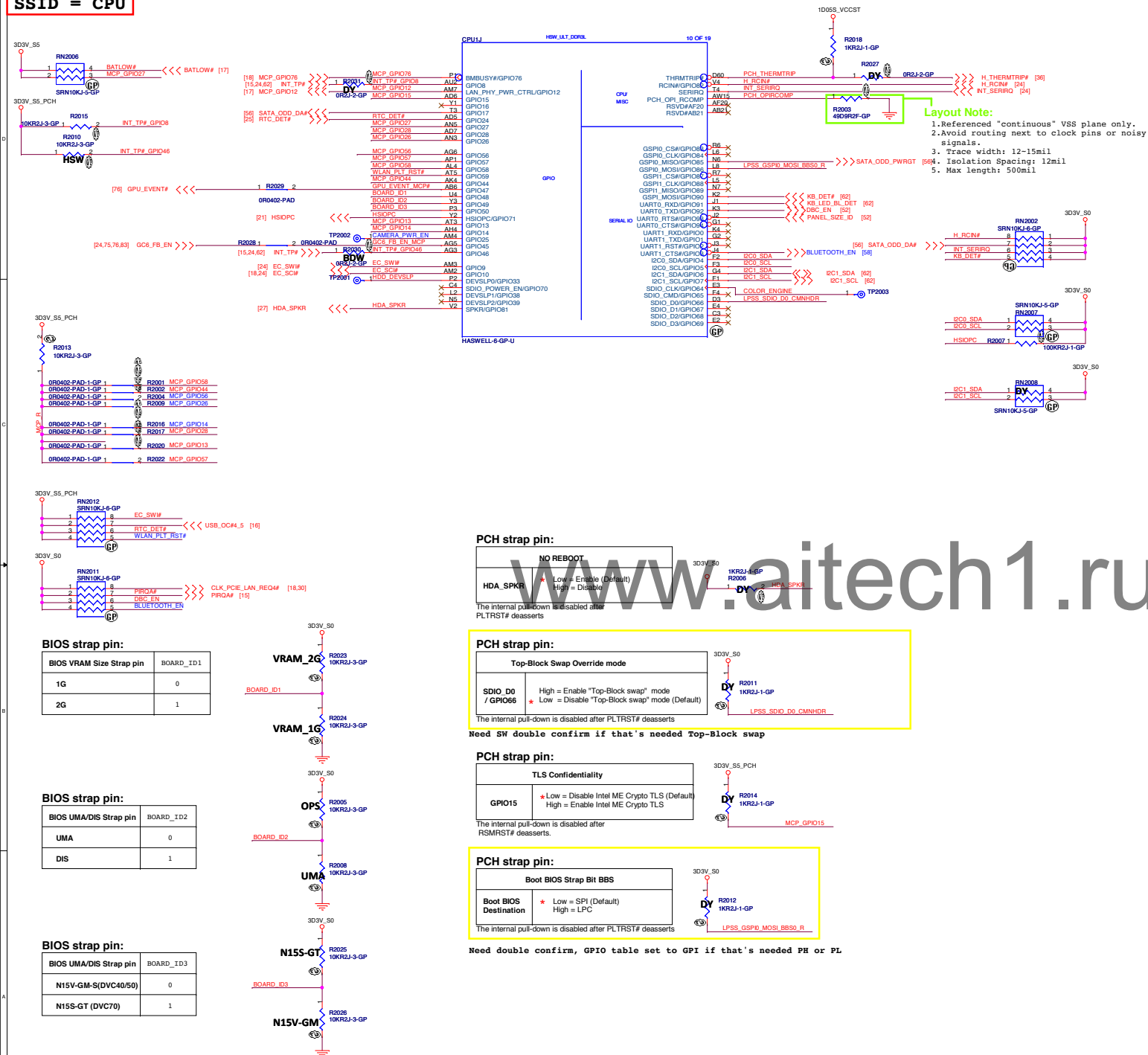
Rev
400

Date: Friday, February 07, 2014

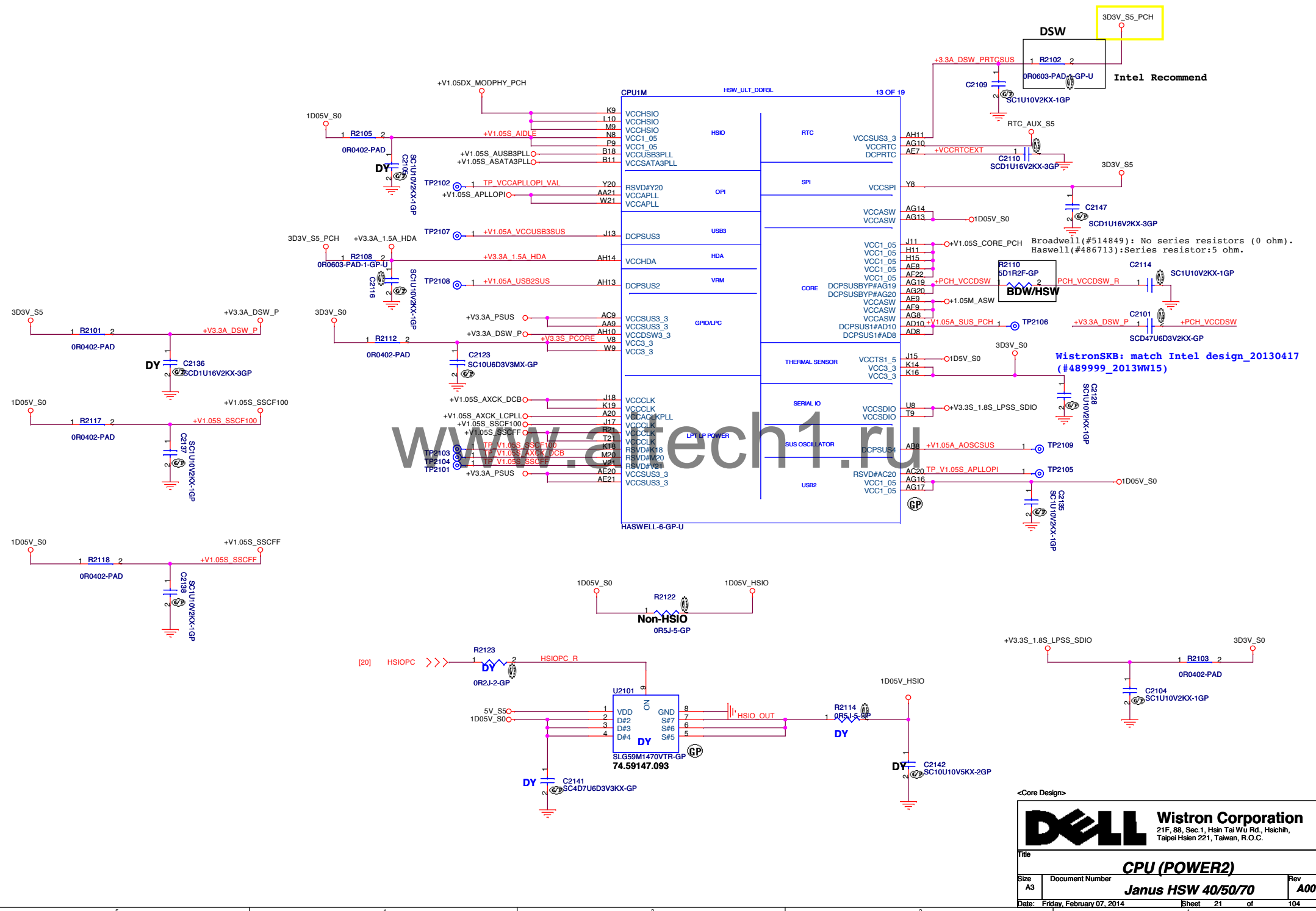
Sheet 19 of 104

104

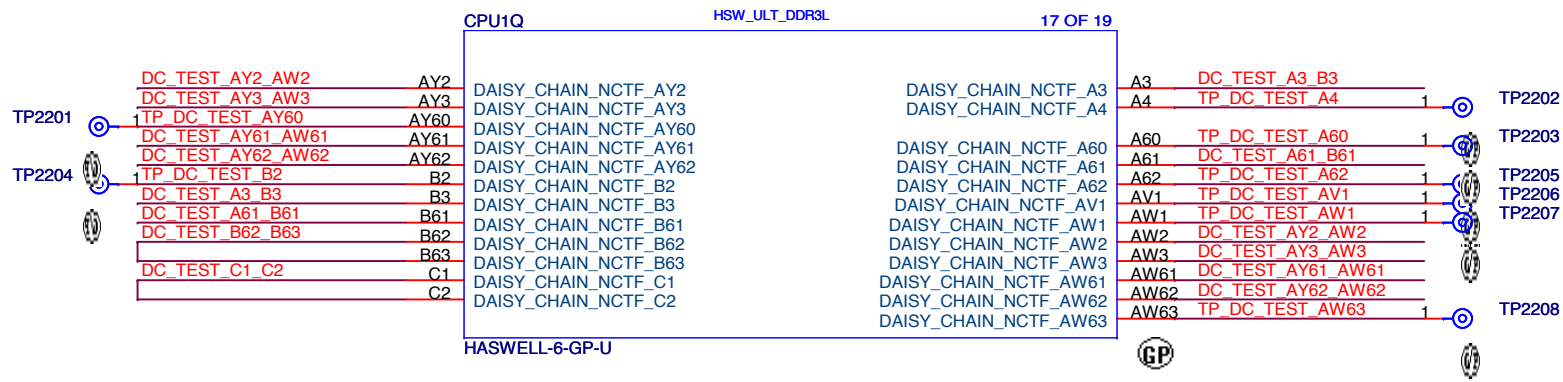
SSID = CPU




SSID = CPU



SSID = PCH



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Title

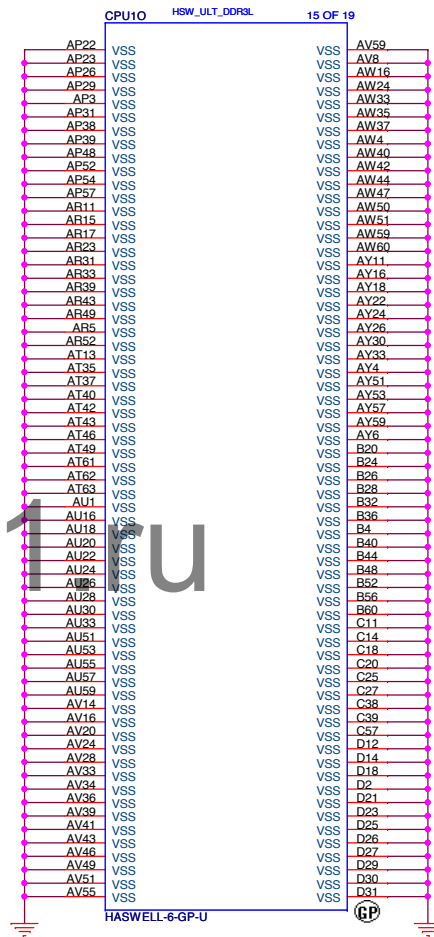
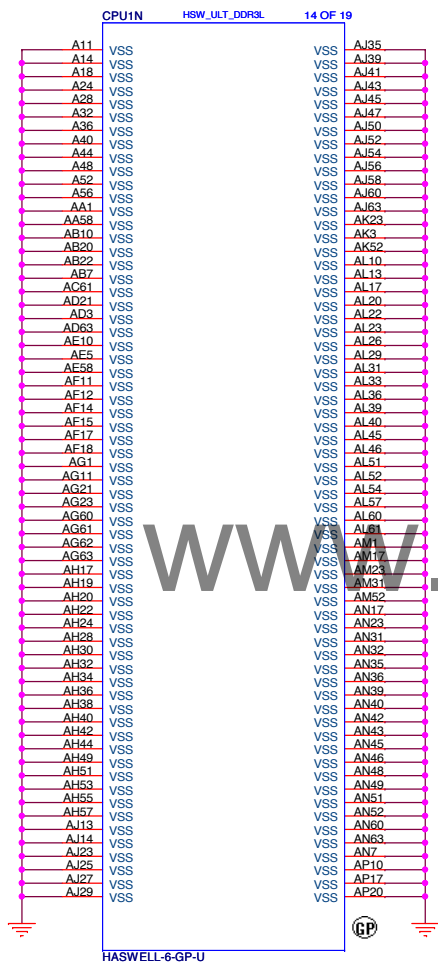
CPU (RSVD)

Size A4	Document Number Janus HSW 40/50/70	Rev A00
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Date: Friday, February 07, 2014

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SSID = PCH



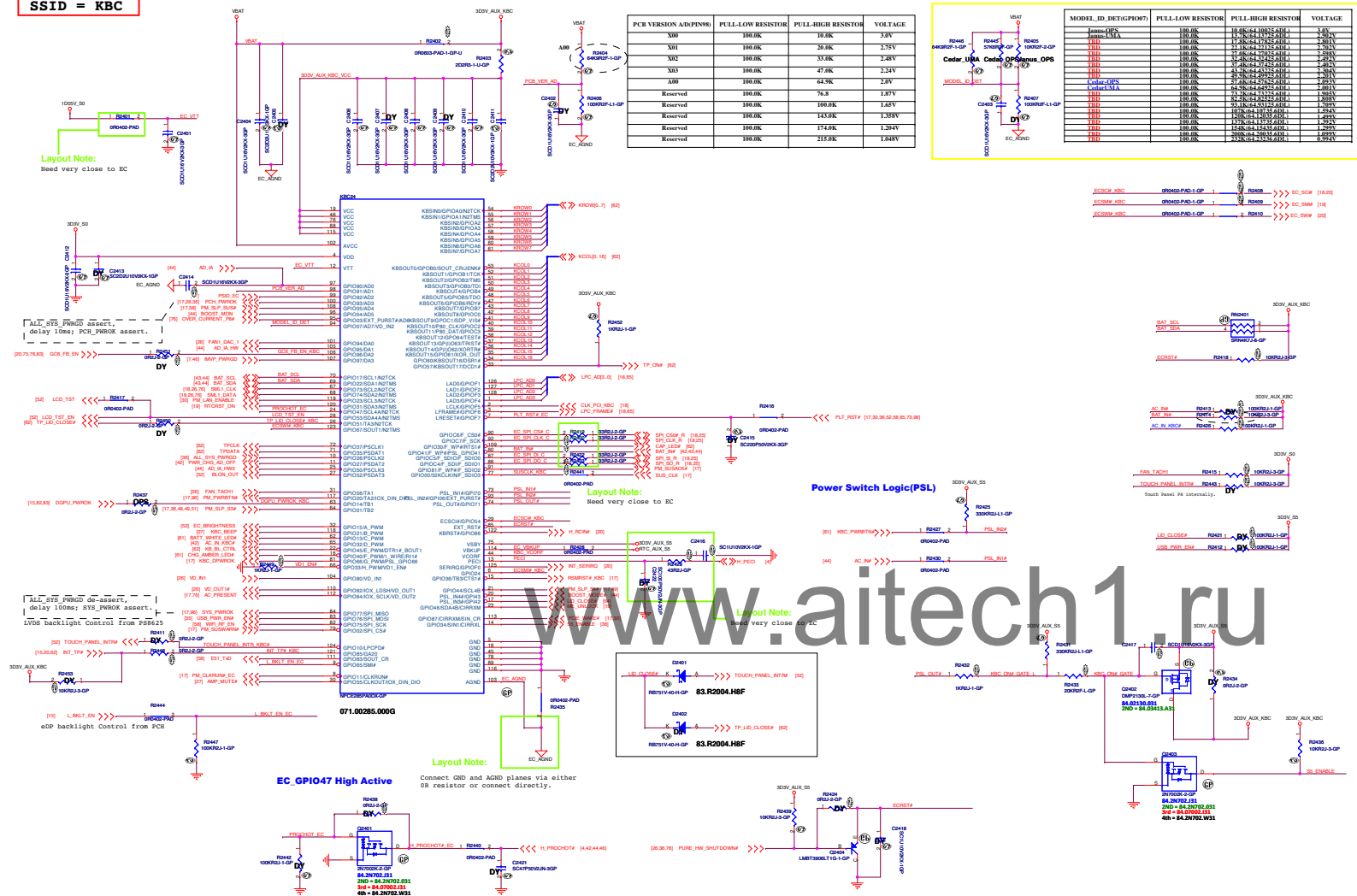
<Core Design>



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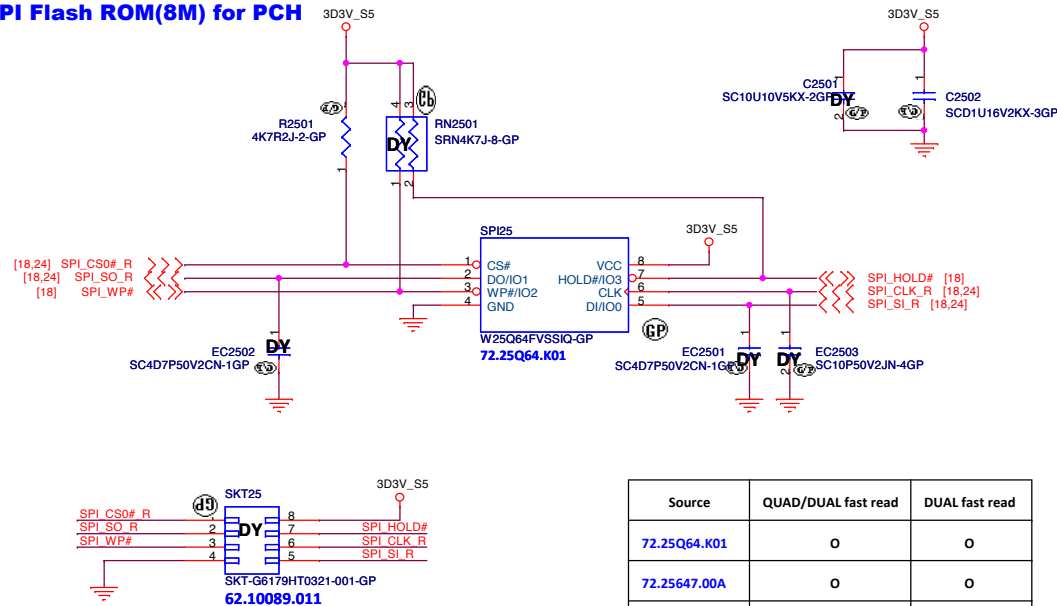
Title			CPU(VSS)	
Size	Document Number	Janus HSW 40/50/70		Rev
A3				A00
Date:	Friday, February 07, 2014	Sheet	23	of 104

SSID = KBC



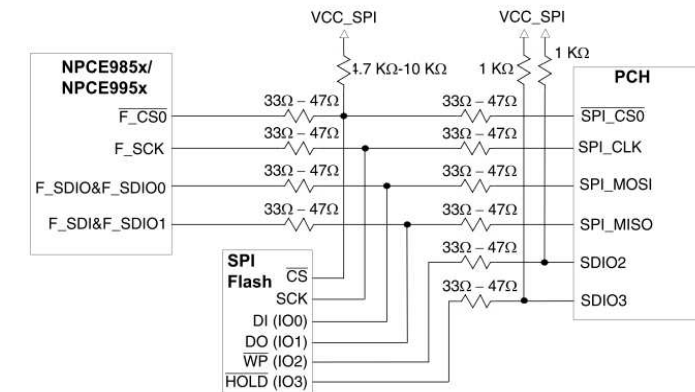
SSID = Flash.ROM

SPI Flash ROM(8M) for PCH



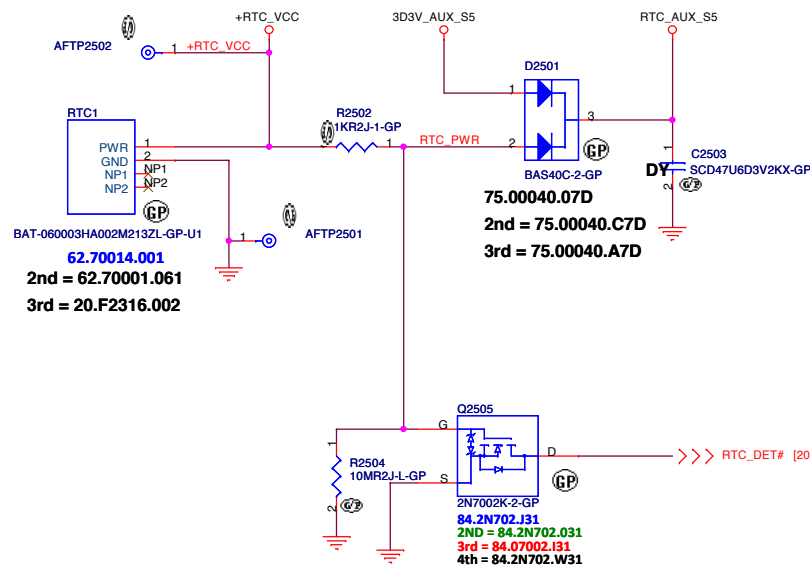
Source	QUAD/DUAL fast read	DUAL fast read
72.25Q64.K01	O	O
72.25647.00A	O	O
072.25B64.0001	O	O

Single SPI shared flash connection (SPI Quad I/O mode)



Refer to "NCPE985x/ NPCE995x board design reference guide"

SSID = RBATT



<Core Design>

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Title

Flash/RTCSize
A3

Document Number

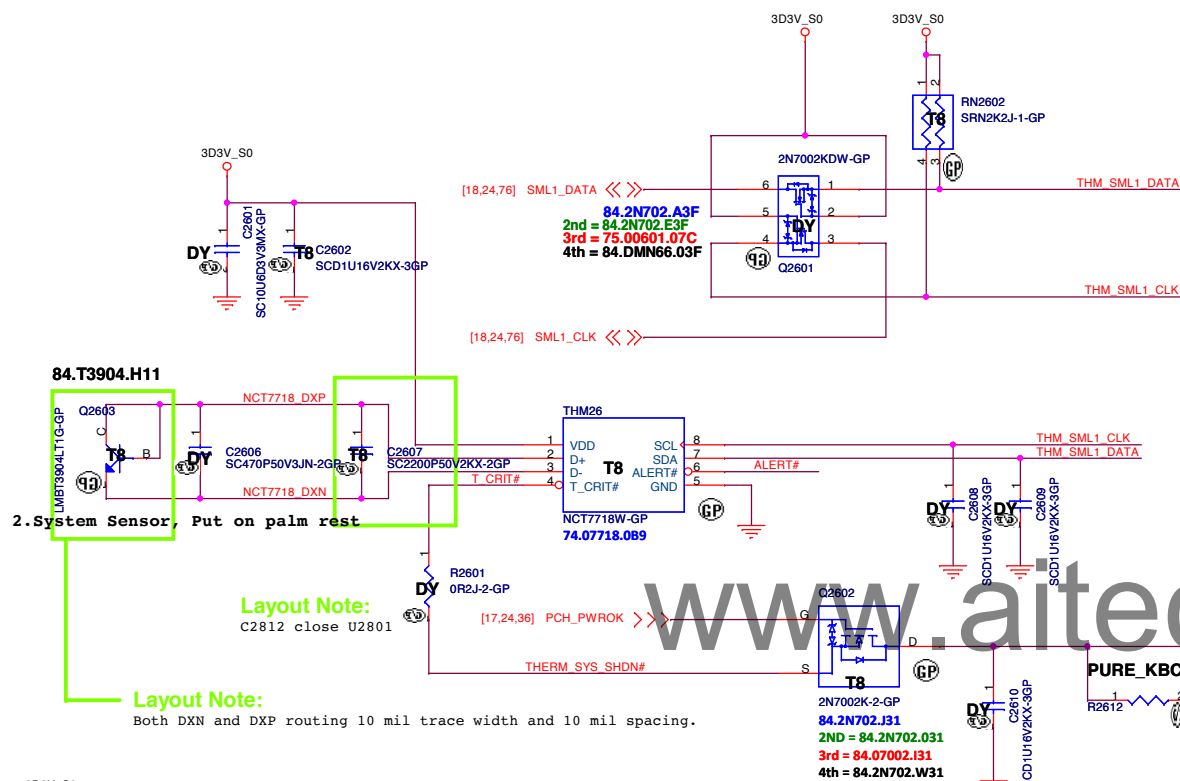
Janus HSW 40/50/70

Rev
A00

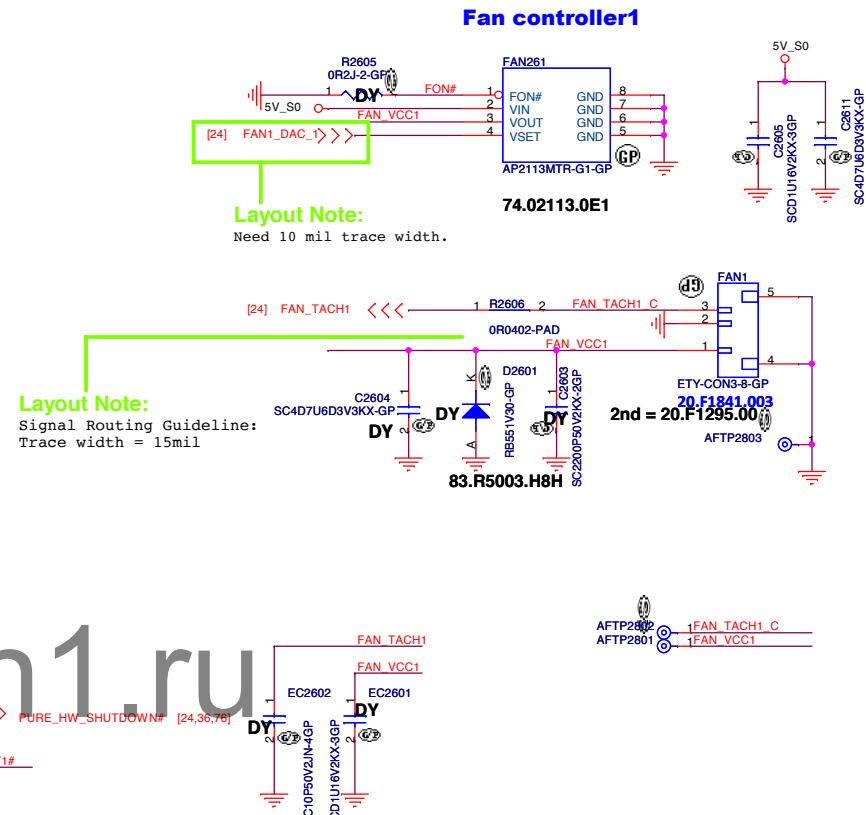
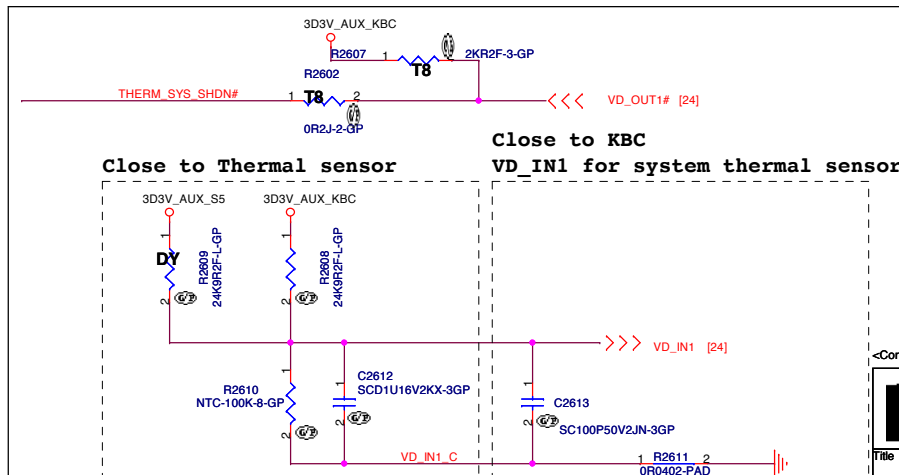
Date: Friday, February 07, 2014

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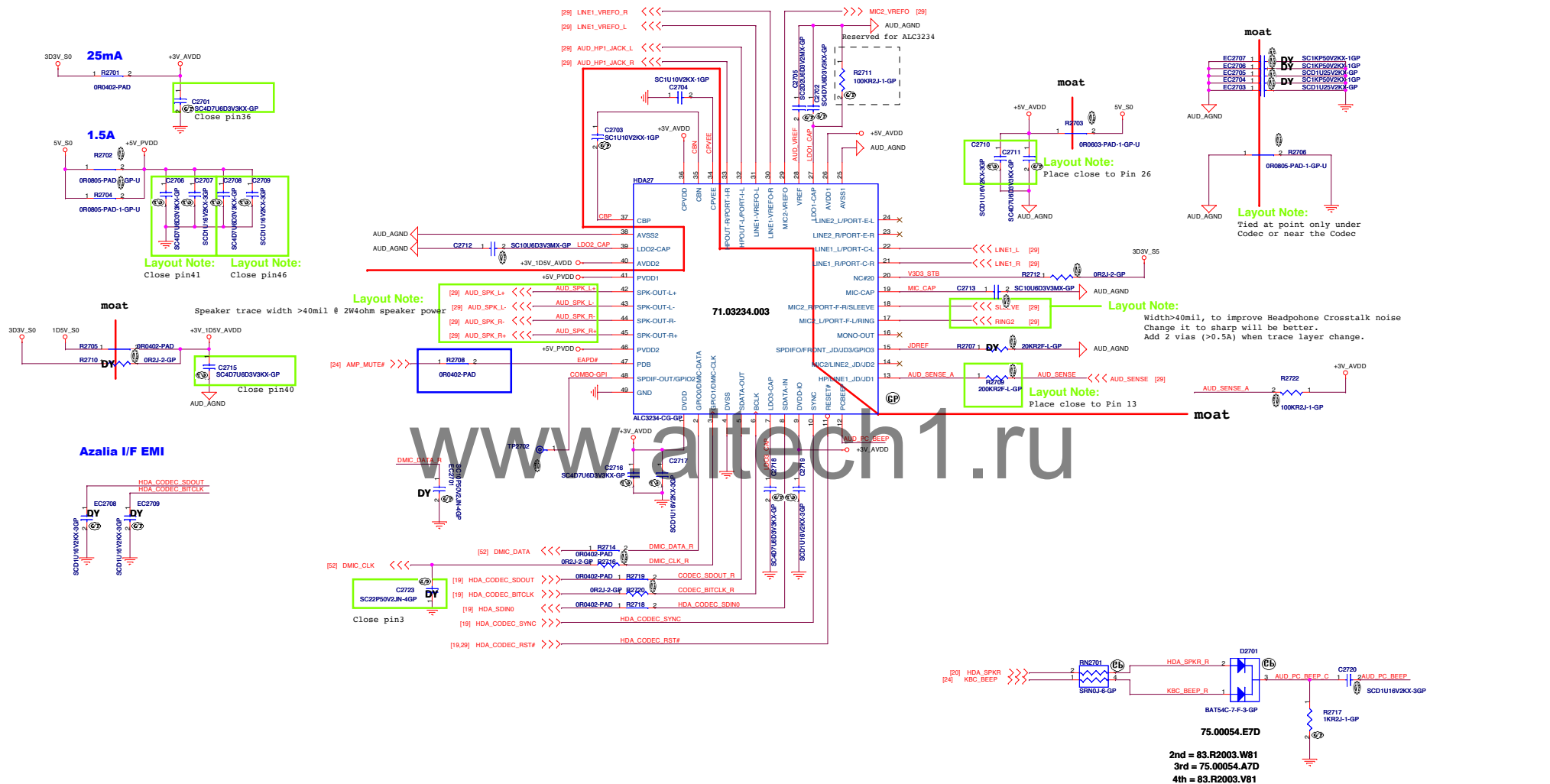
SSID = Thermal



TEMPERATURE (°C)	T_CRIT#					
	2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ	
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125



SSID = AUDIO



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<Core Design>



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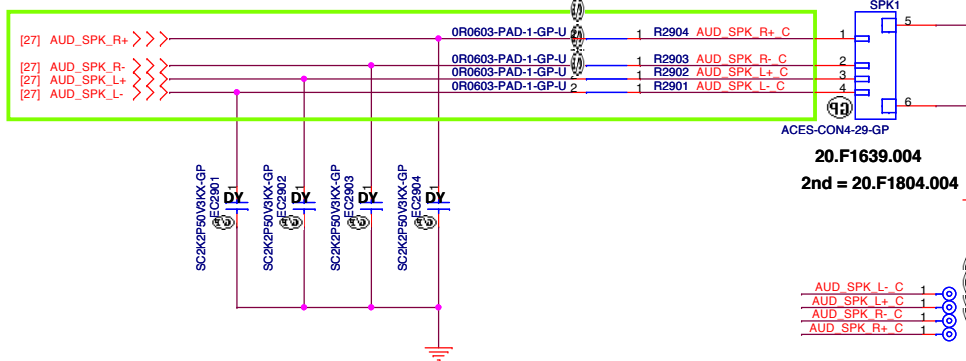
Sheet 28 of 104

SSID = AUDIO

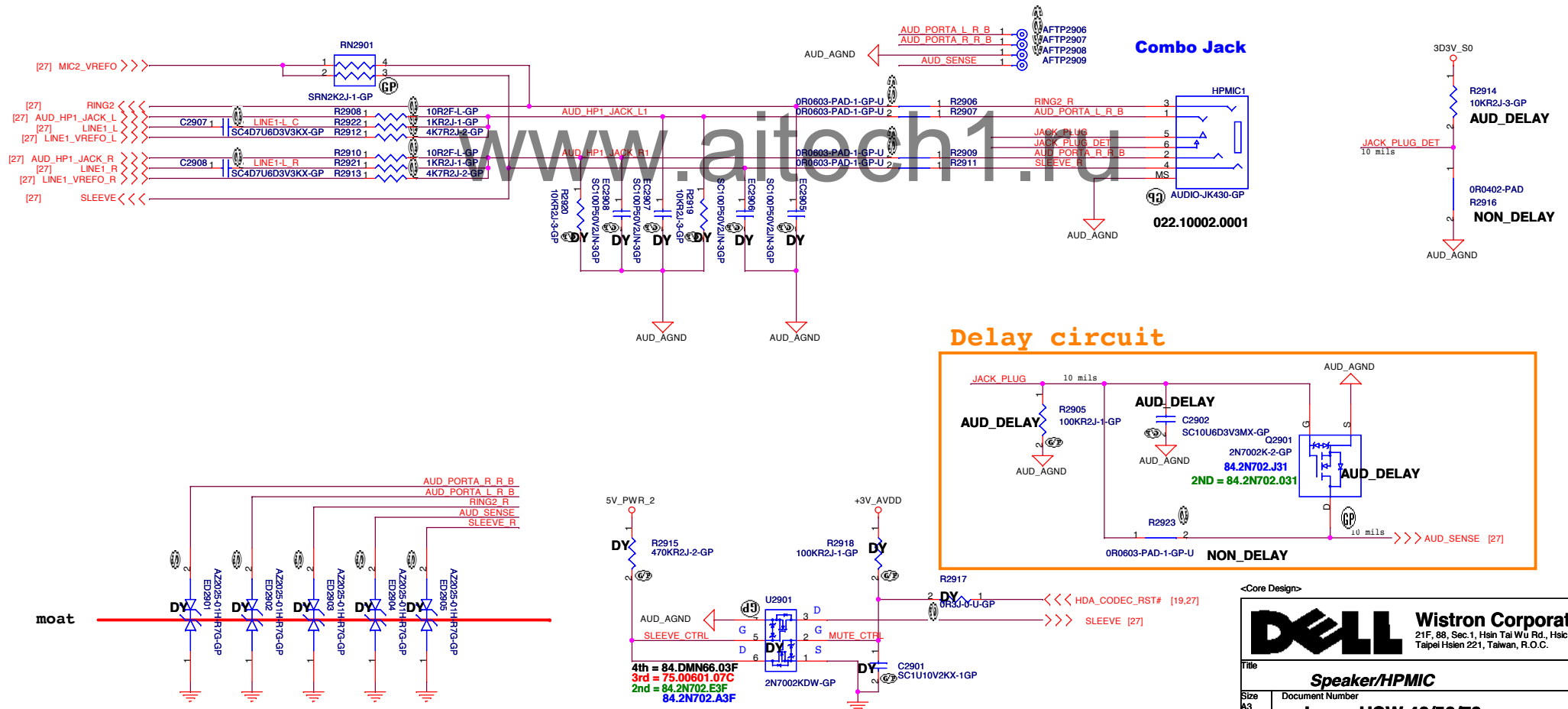
Layout Note:

Speaker trace width >40mil @ 2W4ohm speaker power

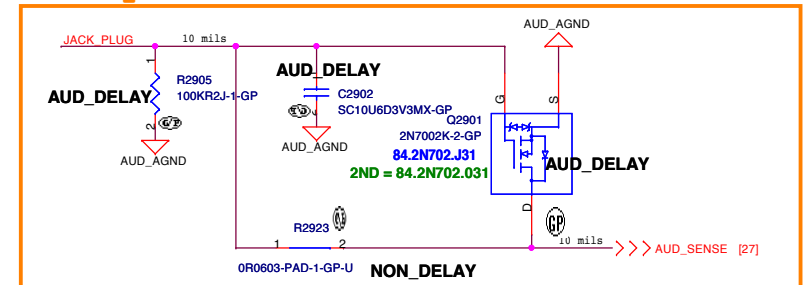
Speaker



CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-



Delay circuit



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Date: Friday, February 07, 2014

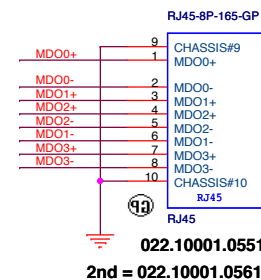
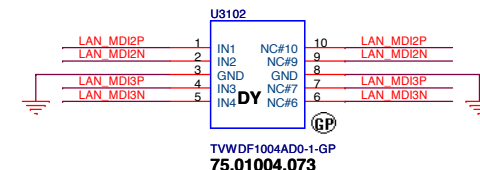
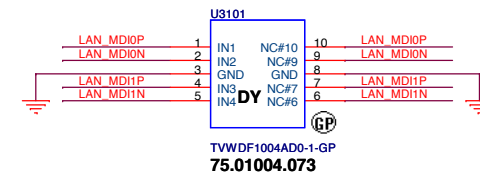
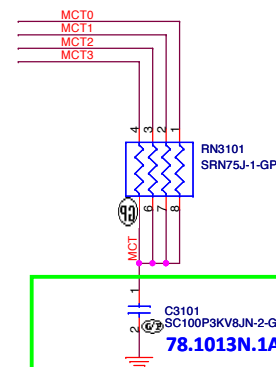
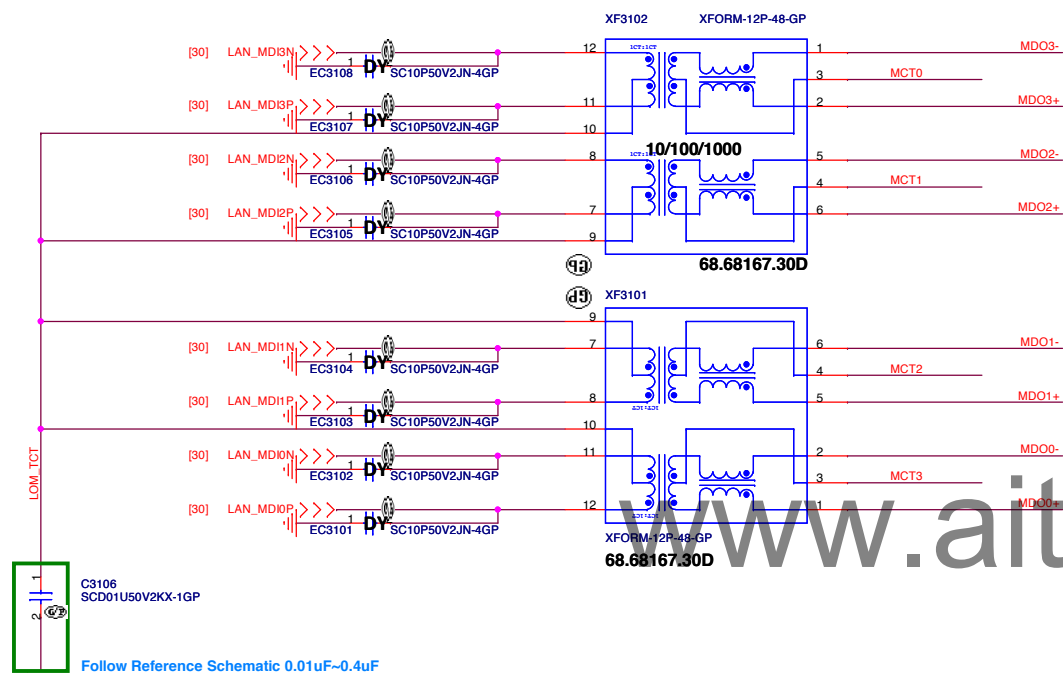
Sheet 29 of 104

SSID = LOM

LAN TransFormer (10/100/1000M & 10/100M co-lay)

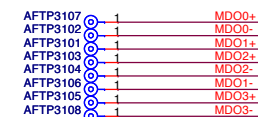
Layout note:

30 mil spacing between MDI differential pairs.



Layout:

Place near RJ45



<Core Design>



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XFOM&RJ45

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<Core Design>



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<Core Design>



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Size
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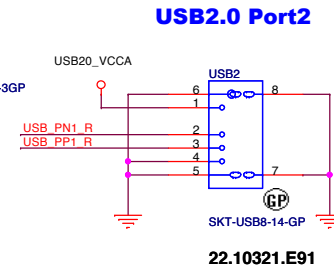
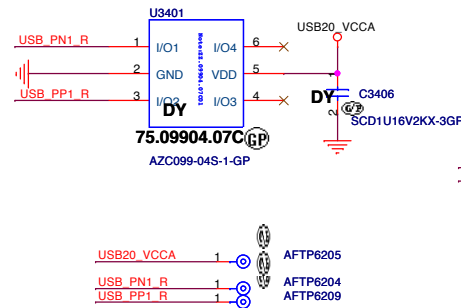
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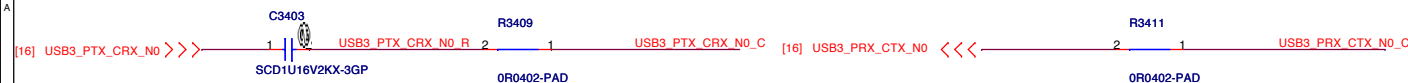
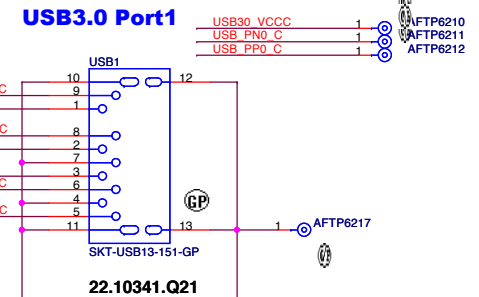
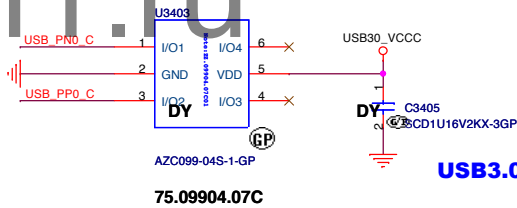
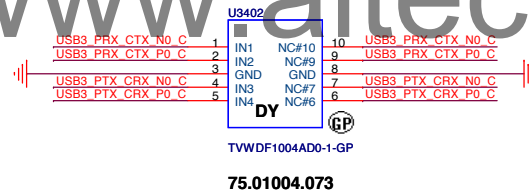
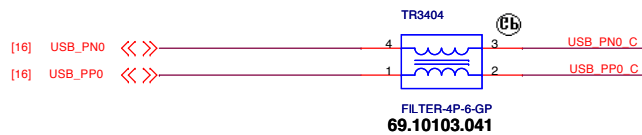
Date: Friday, February 07, 2014

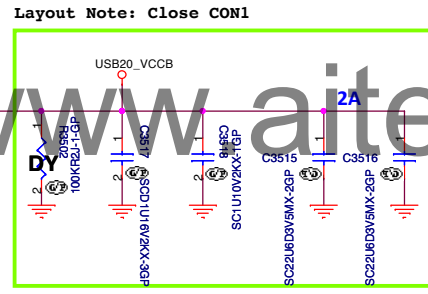
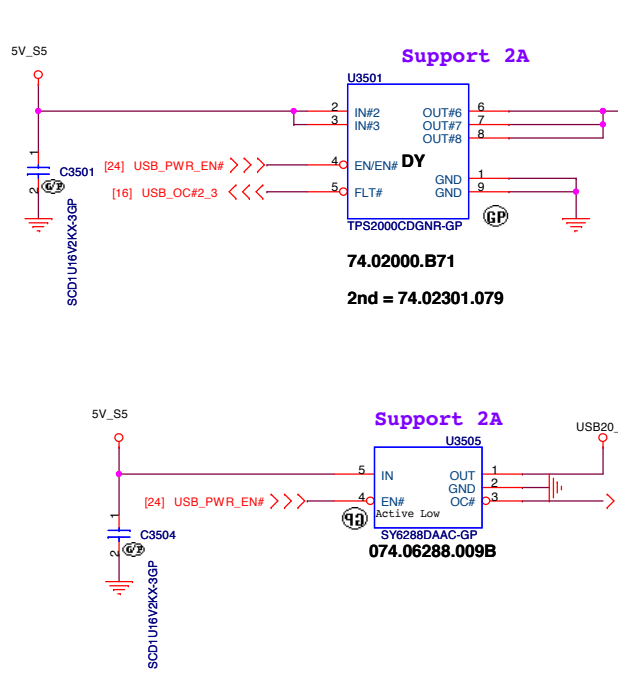
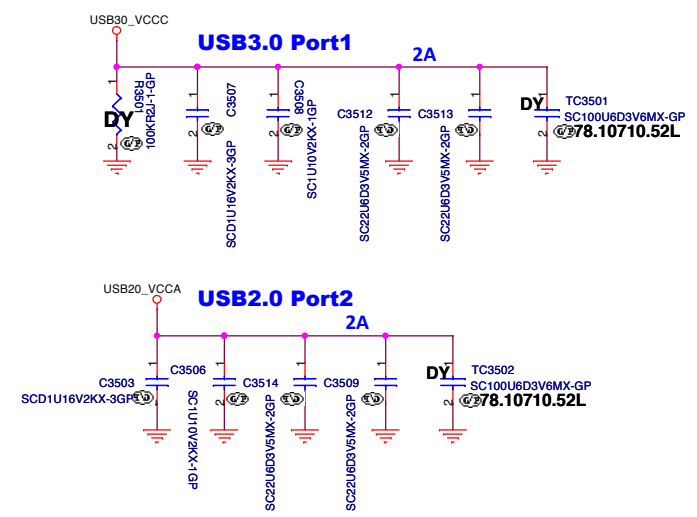
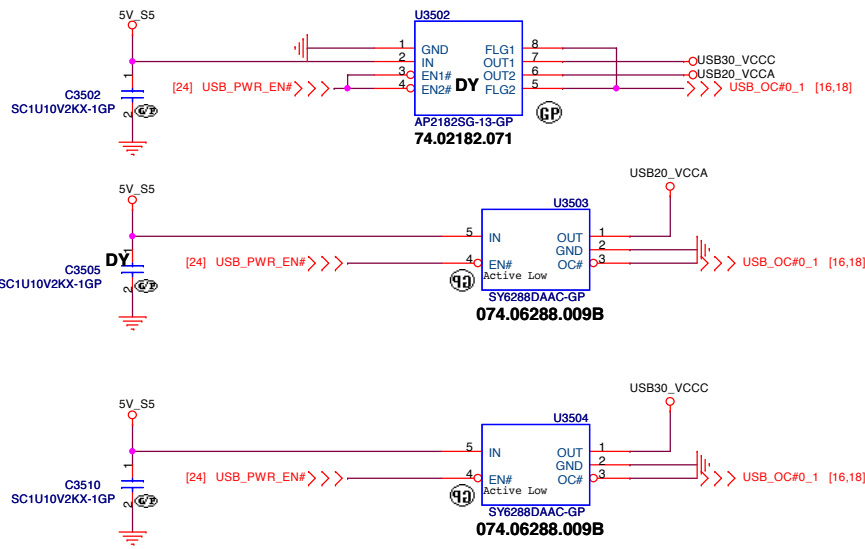
Sheet 33 of 104

SSID = USB



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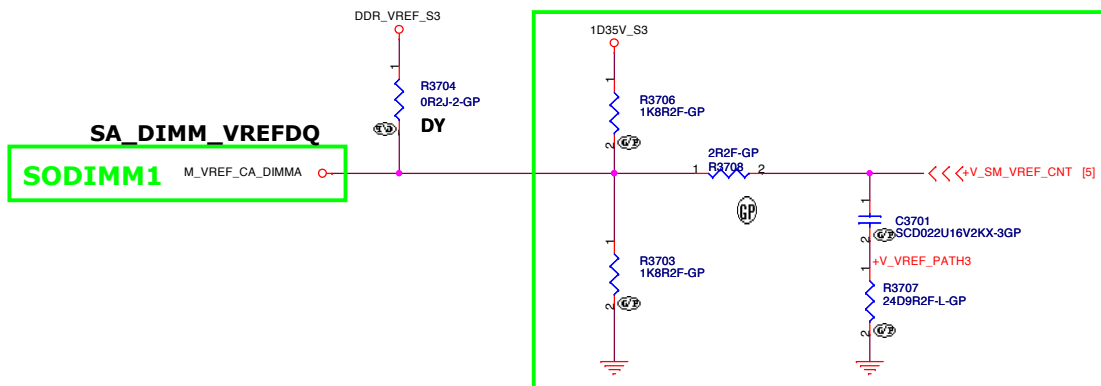


Layout Note: Close CON1

SSID = Reset.Suspend

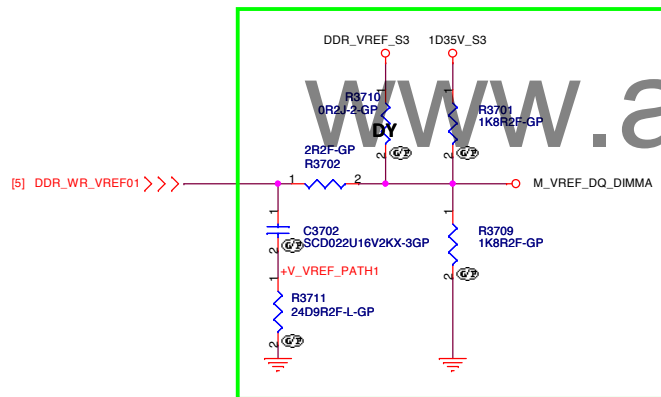
Layout Note:

Place Close SO-DIMM1



Layout Note:

Place Close SO-DIMM1



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S3 Reduction Circuit

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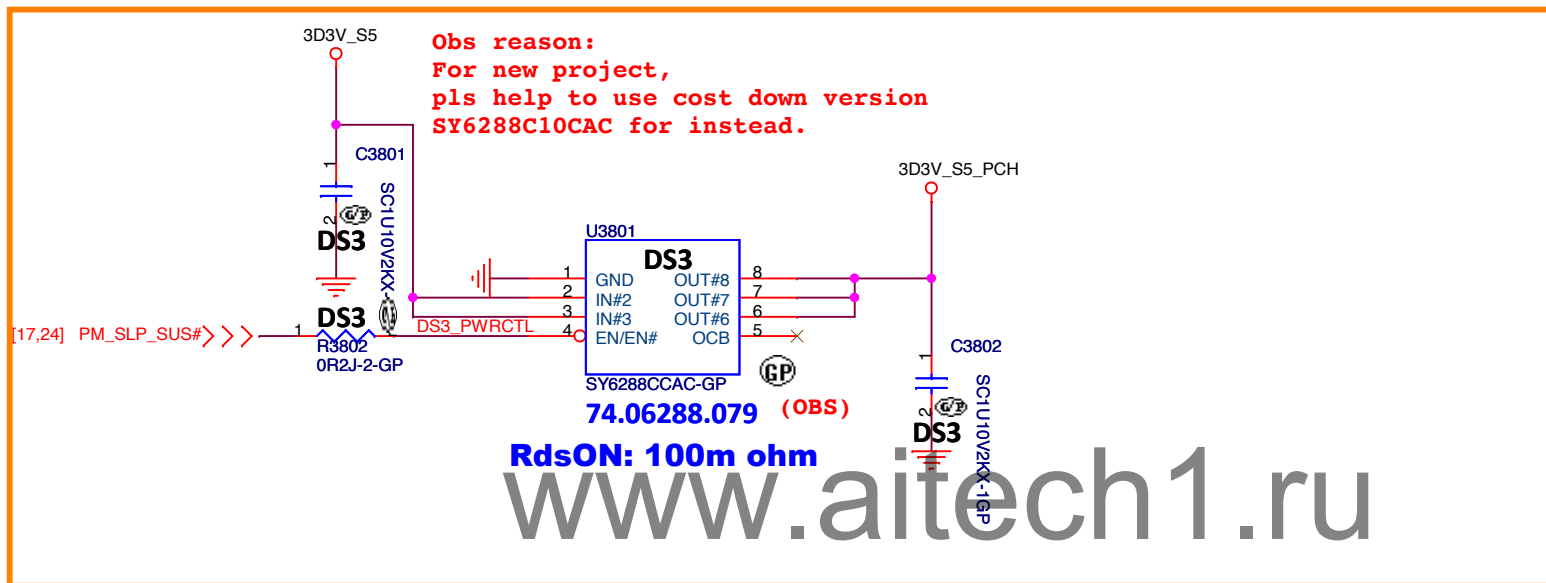
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Obs reason:
For new project,
pls help to use cost down version
SY6288C10CAC for instead.



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Title			DSW	
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Title

(Reserved) 1D05_M

Size
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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
<i>Reserved</i>		
Size A4	Document Number <i>Janus HSW 40/50/70</i>	Rev <i>A00</i>
Date: Friday, February 07, 2014		Sheet 40 of 104

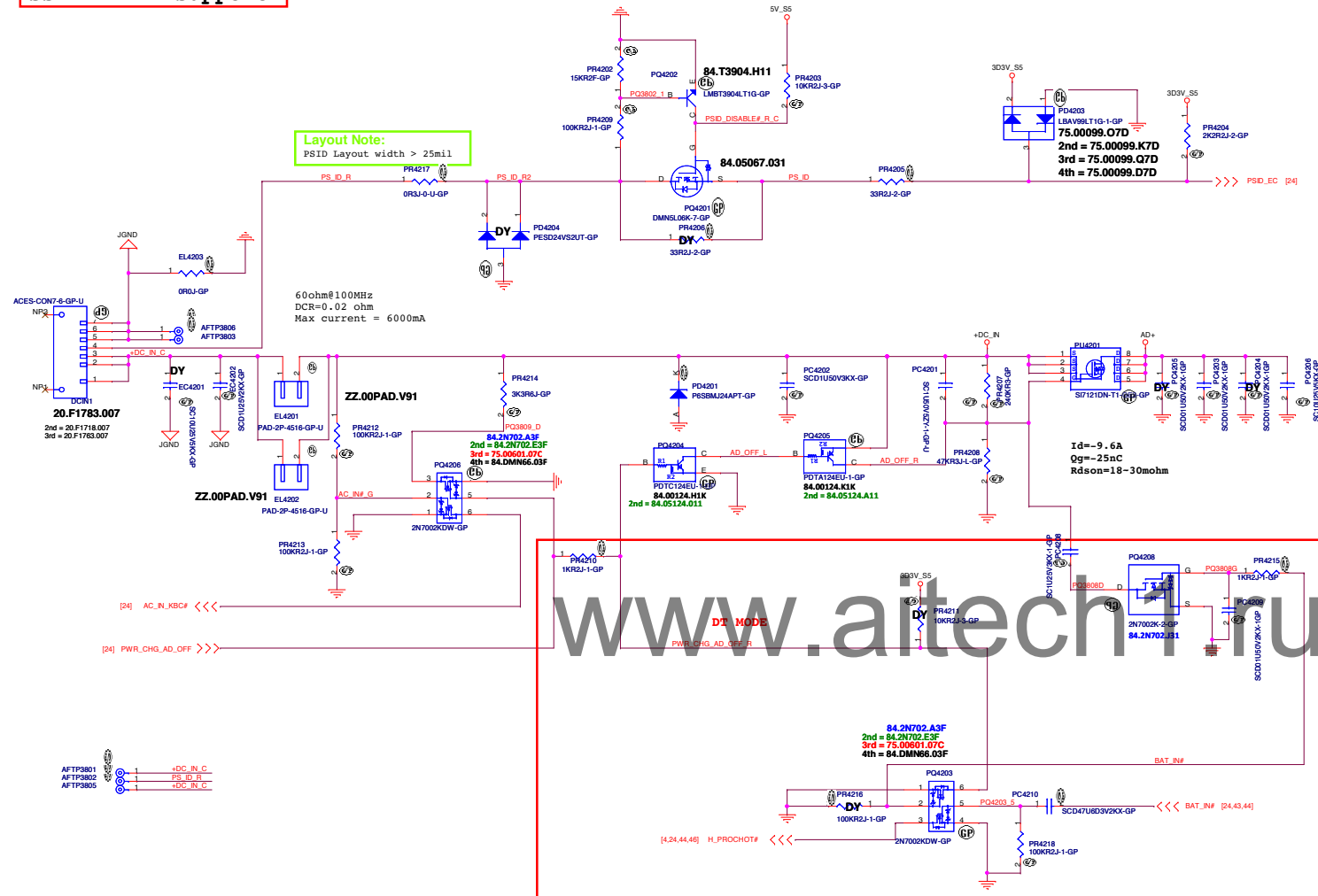
(Blanking)

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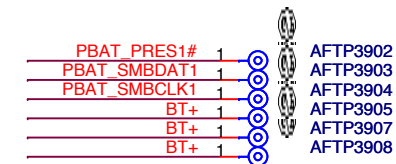
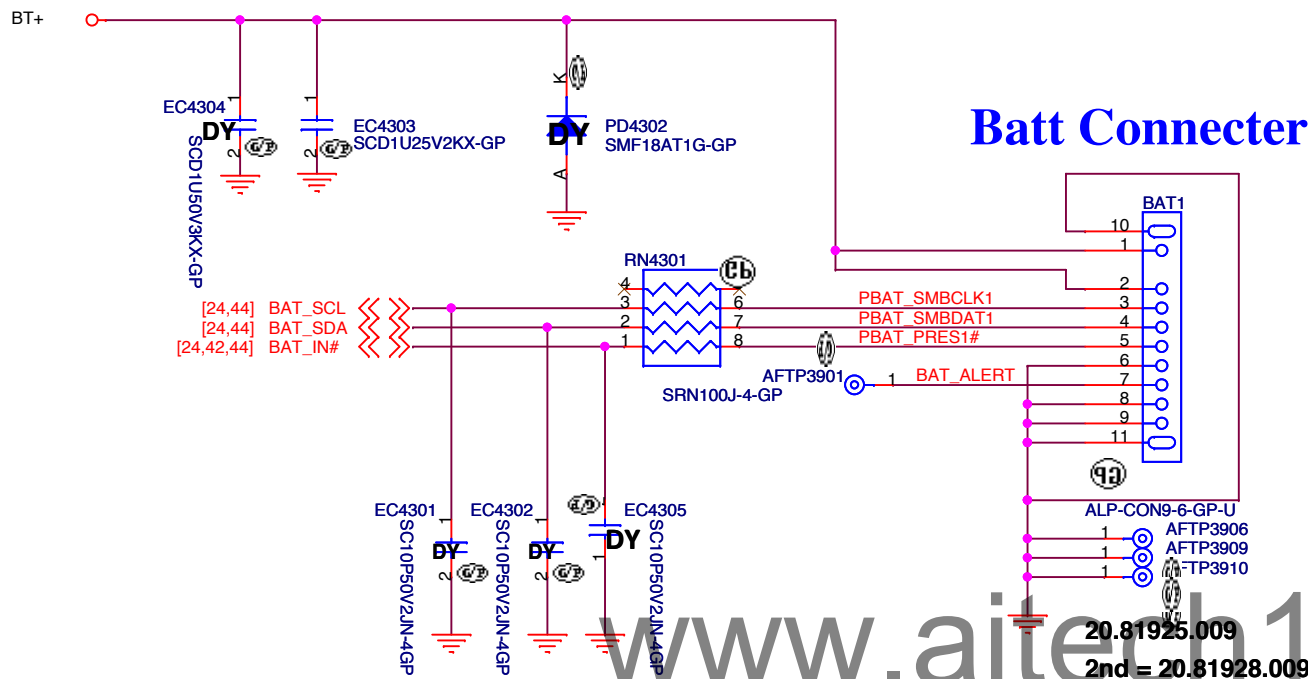
<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<i>Reserved</i>			
Size A4	Document Number <i>Janus HSW 40/50/70</i>		Rev <i>A00</i>
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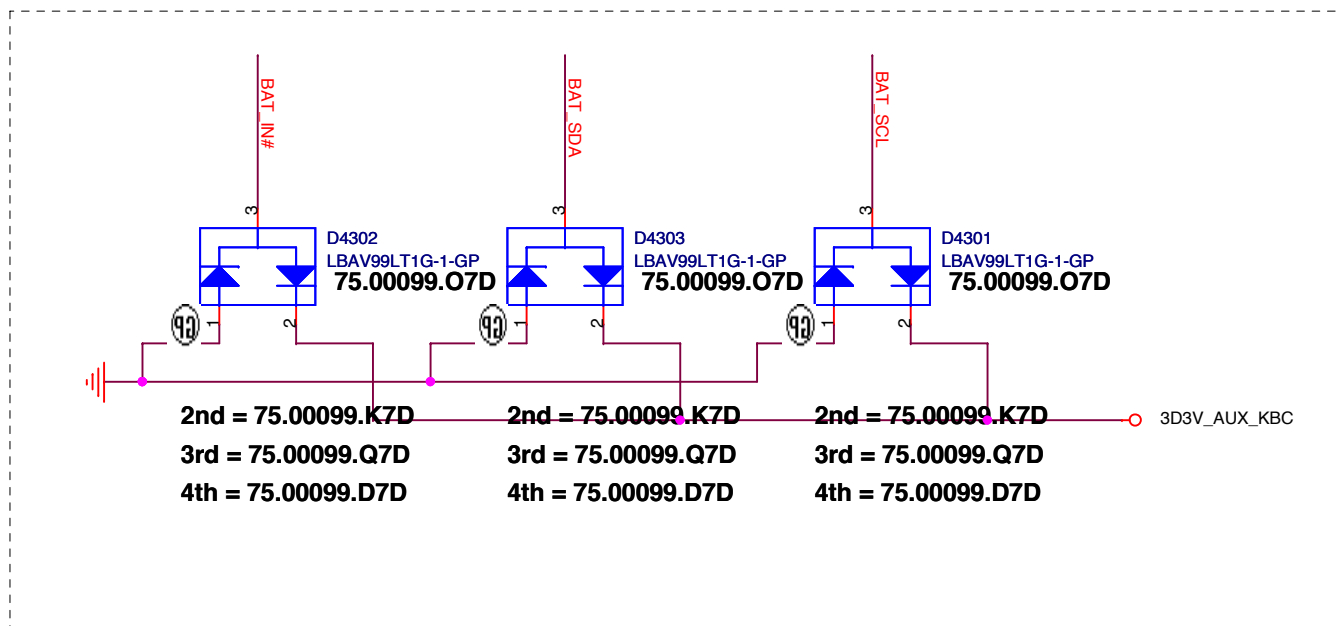
SSID = PWR.Support



SSID = PWR.Support



Placement: Close to Batt Connector



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BATT CONN

Size
A4

Document Number

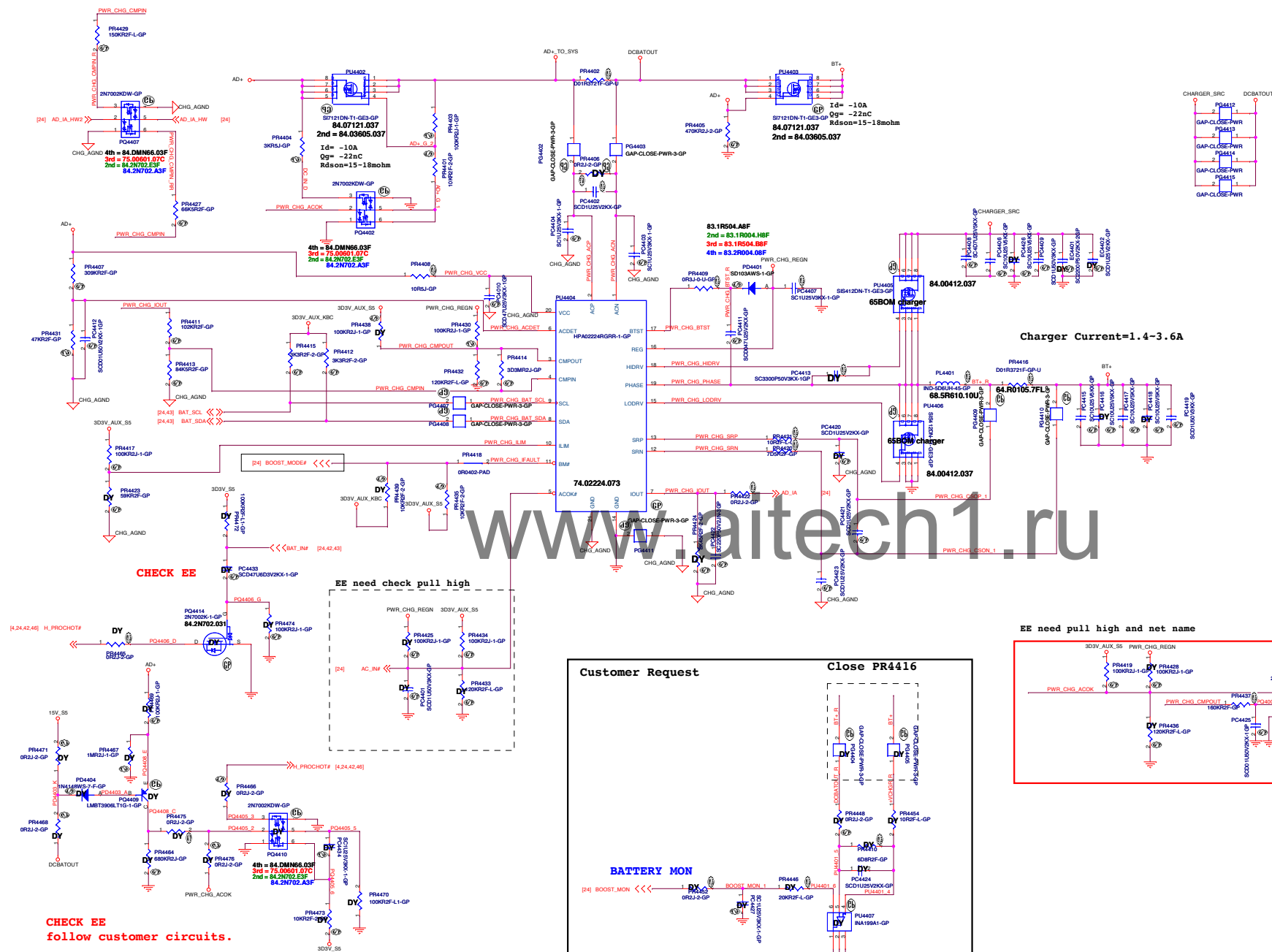
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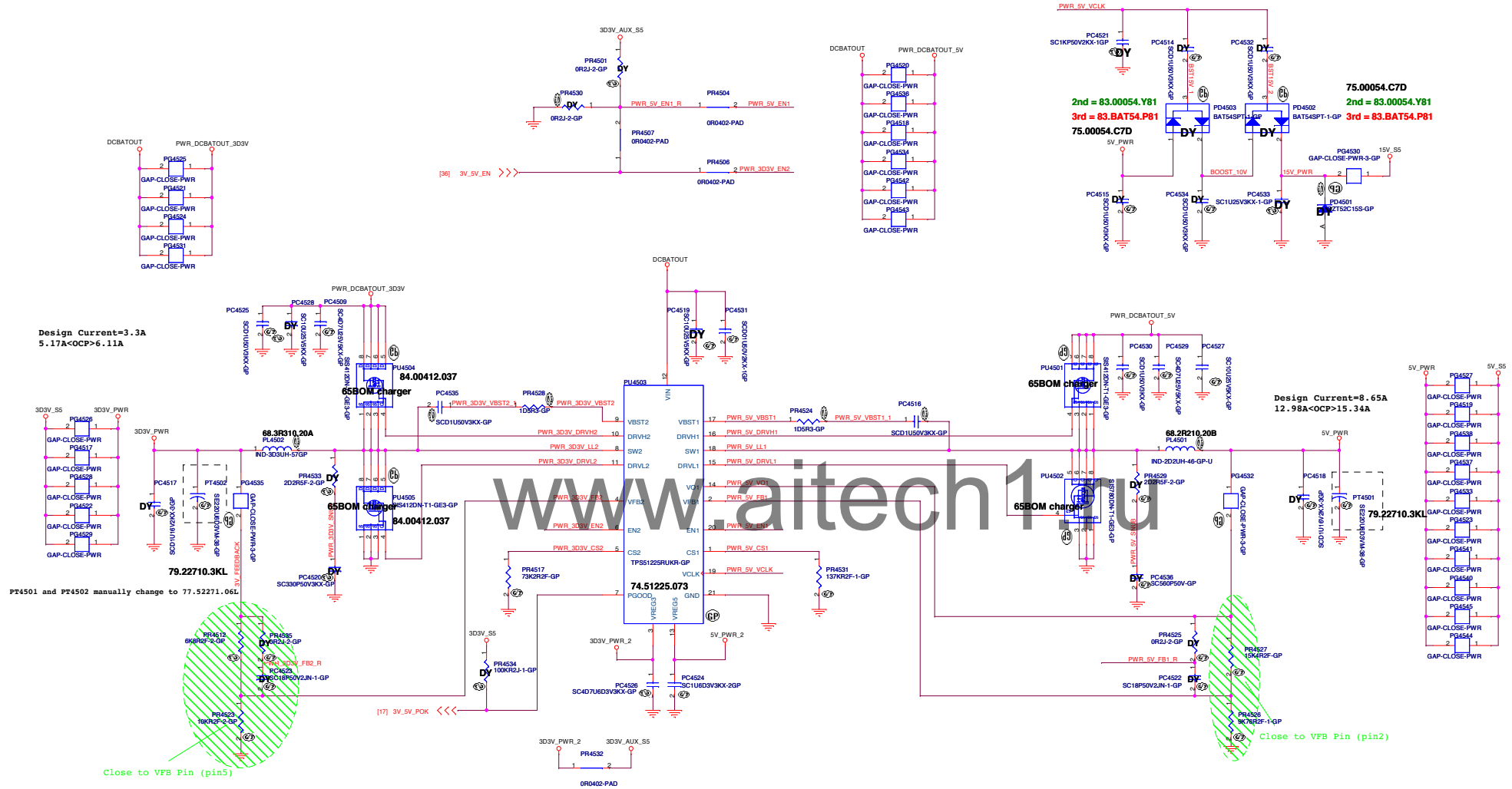
SSID = Charger



EC code only B024707

H_PROCHOT#	AD_IA_HW	AD_IA_H
45W	0	0
65W	1	0
90W	0	1

SSID = PWR.Plane.Regulator_5v3p3v



Design Current=3.3A
5.17A<OCP>6.11A

Design Current=8.65A
12.98A<OCP>15.34A

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 3.3UH PCMC063T-3R3MN Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
O/P cap:CHIP CAP POL 220U 6.3V M 6.3*4.5 /Matsuki/ 17mohm / 77.52271.09L
H/S:SIS412 / 24mohm/30mohm4.5Vgs / 84.00412.037
L/S:SIS780 / 14.5mohm/17.5mohm4.5Vgs / 84.00780.037

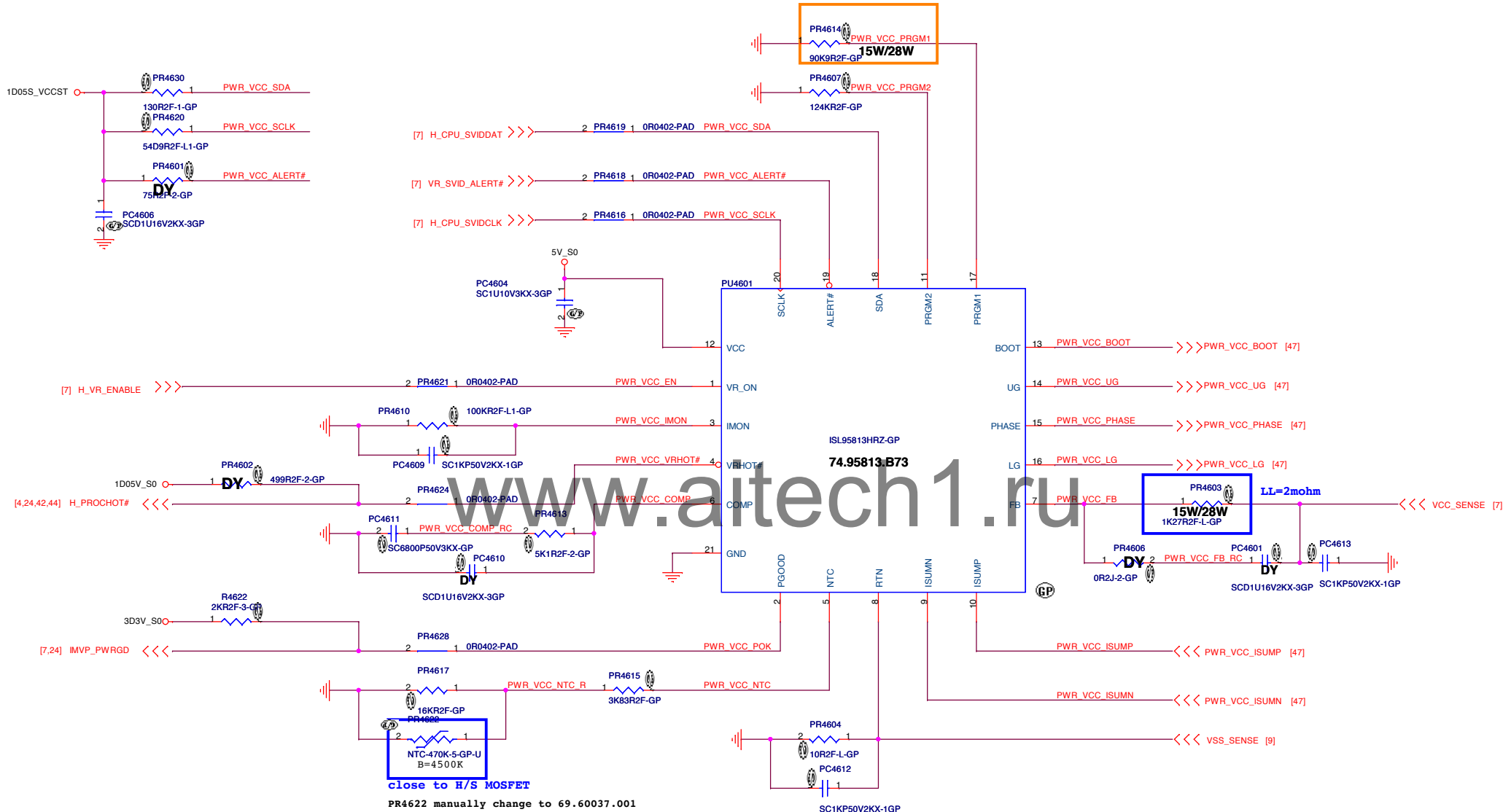
TPS51225 & TPS51285 Co-Lay

	TPS51225	TPS51285
PR4510	45.3KK	9.09K
PR4511	110K	22.1K

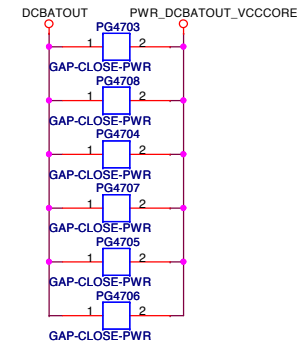
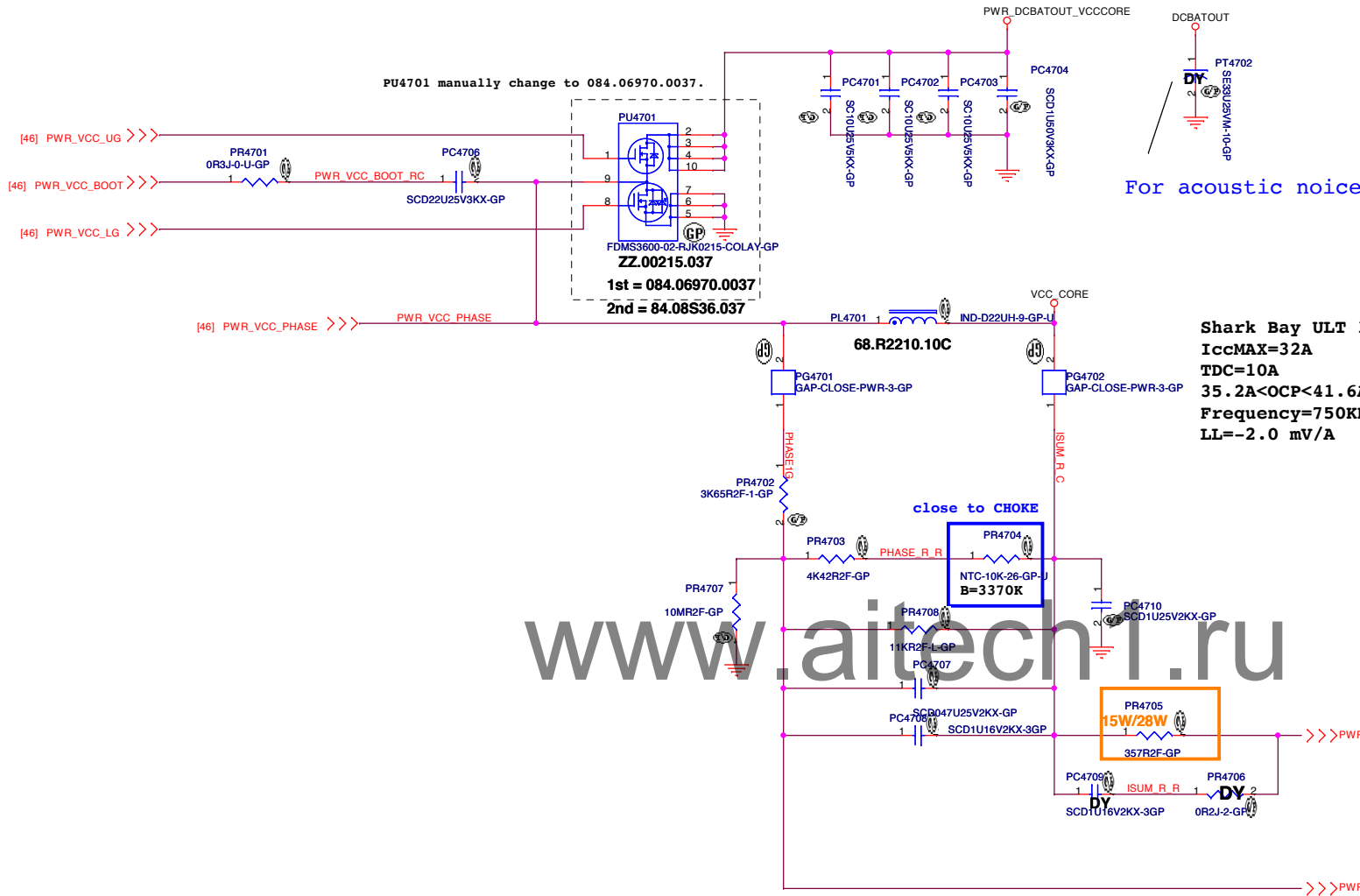
I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOK 2.2U PCMC063T-2R2MN 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P cap:CHIP CAP POL 220U 6.3V M 6.3*4.5 /Matsuki/ 17mohm / 77.52271.09L
H/S:SIS412 / 24mohm/30mohm4.5Vgs / 84.00412.037
L/S:SIS780 / 14.5mohm/17.5mohm4.5Vgs / 84.00780.037

<Core Design>

SSID = CPU.Regulator



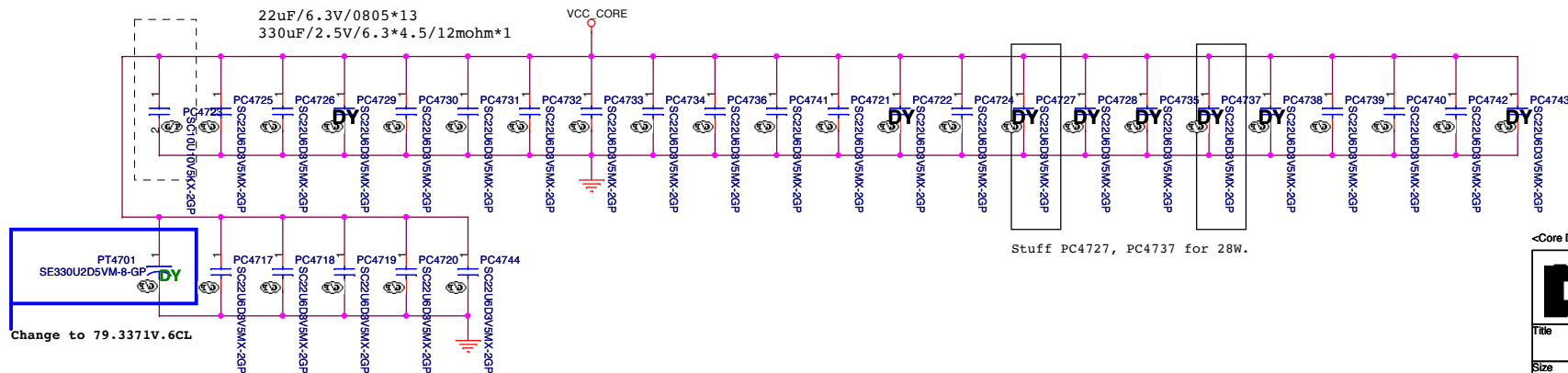
	PR4603	PR4614
15W	1.27K 64.12715.6DL	90.9K 64.90925.6DL
28W	1.58K 64.15815.6DL	113K 64.11335.6DL



Shark Bay ULT 15W CPU
IccMAX=32A
TDC=10A
35.2A<OCP<41.6A
Frequency=750KHZ
LL=-2.0 mV/A

	PR4705 (Cyntec)	OCP
15W	357 ohm (64.35705.6DL)	38A
28W	412 ohm (64.41205.6DL)	48A
	PR4705 (Maglayers)	
15W	383 ohm (64.38305.6DL)	38A
28W	464 ohm (64.46405.6DL)	48A

Change PC4723 to 10U from 22U based on PI Simulation.



<Core Design>

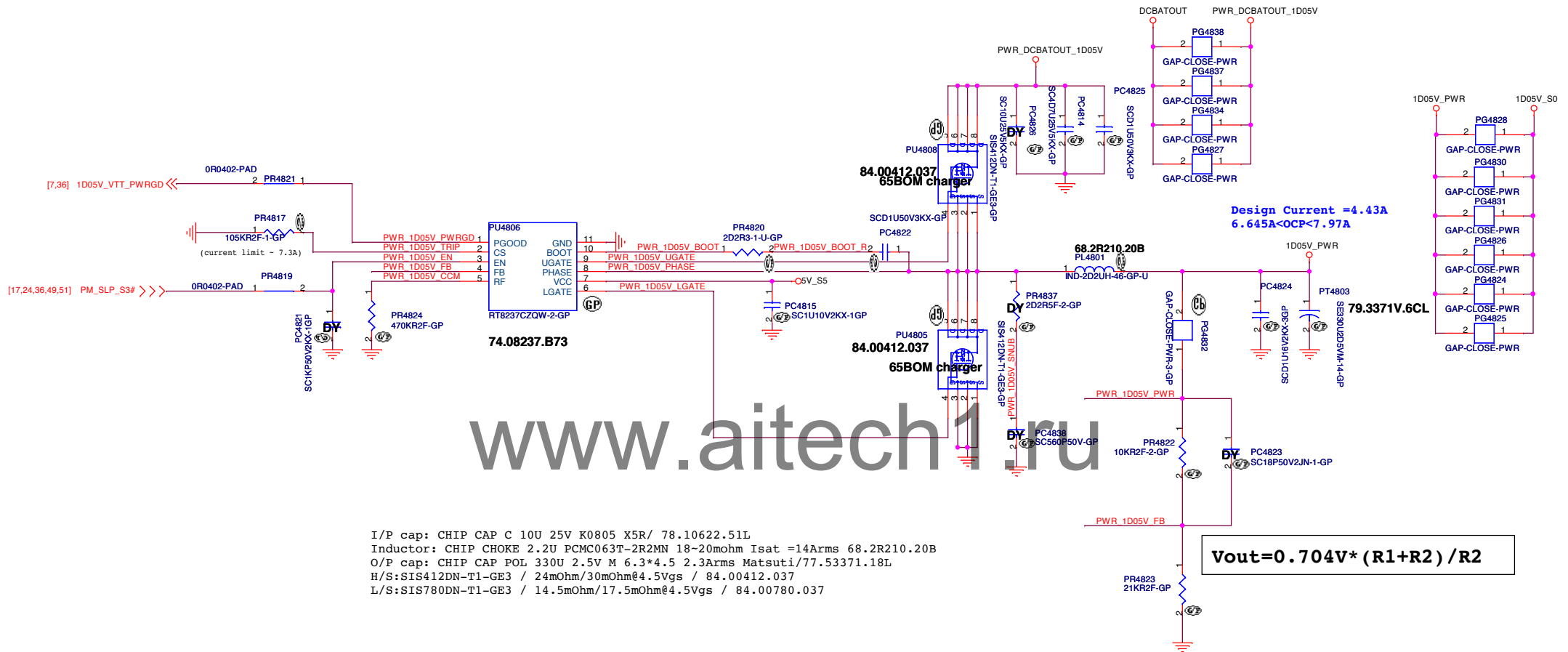
DELL Wistron Corporation
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Title
ISL95813 CPUCORE(2/2)

Size A3 Document Number
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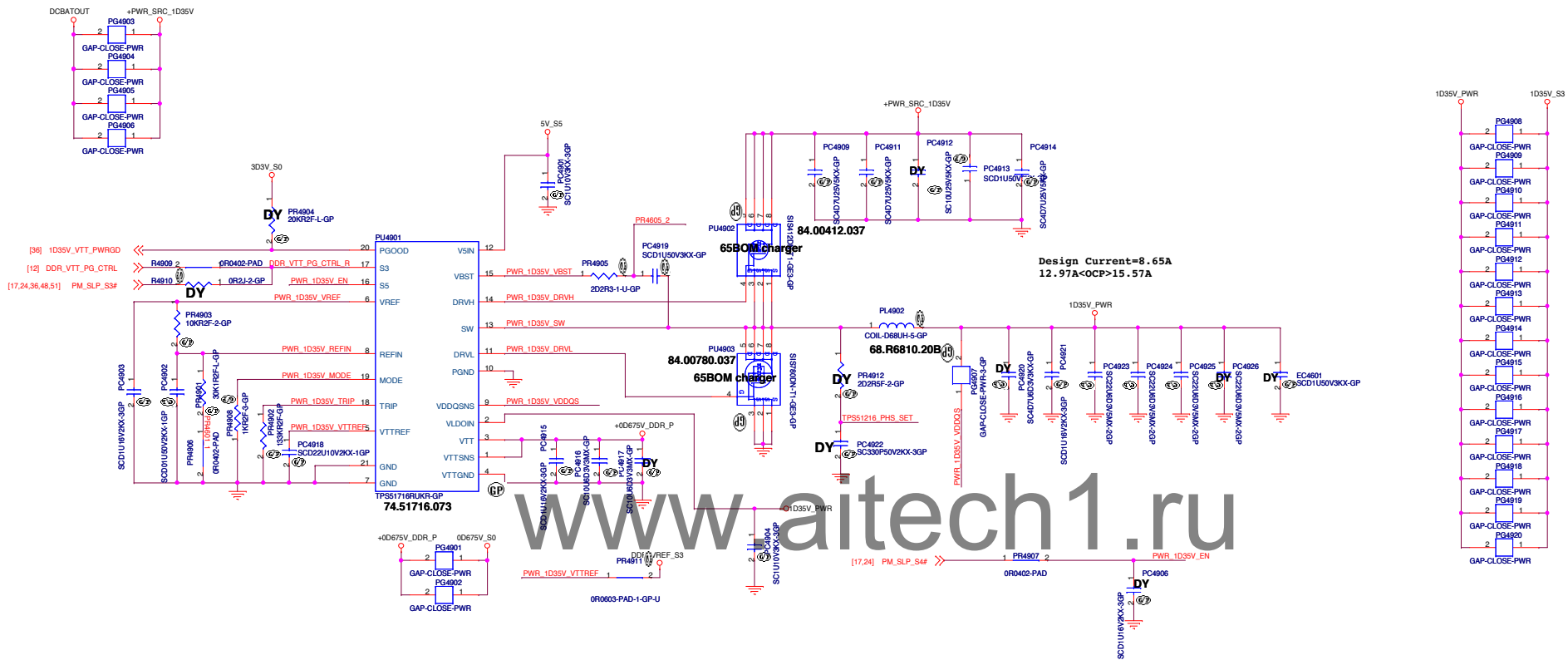
SSID = PWR.Plane.Regulator_1p05v



I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 2.2U PCMC063T-2R2MN 18~20mohm Isat =14Arms 68.2R210.20B
O/P cap: CHIP CAP POL 330U 2.5V M 6.3*4.5 2.3Arms Matsuti/77.53371.18L
H/S:SIS412DN-T1-GE3 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS780DN-T1-GE3 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

<Core Design>

SSID = PWR.Plane.Regulator lp35v0p675v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off


I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
 Inductor: CHIP IND 0.1UH M PCMC0637-R104M 1.5~1.7mohm Isat =60Arms 68.R1010.10T
 O/P cap: CHIP CAP POL 330U 2.5V M 6.3+4.5 2.3Arms Matsuti/77.53371.18L
 MOS: FET MOS FDM3364S NC POWER56 / 84.03664.037 / Q1: 8.5~11mohm @Vgs=4.5V Q2: 2.6~3.2mohm @Vgs=4.5V

<Core Design>

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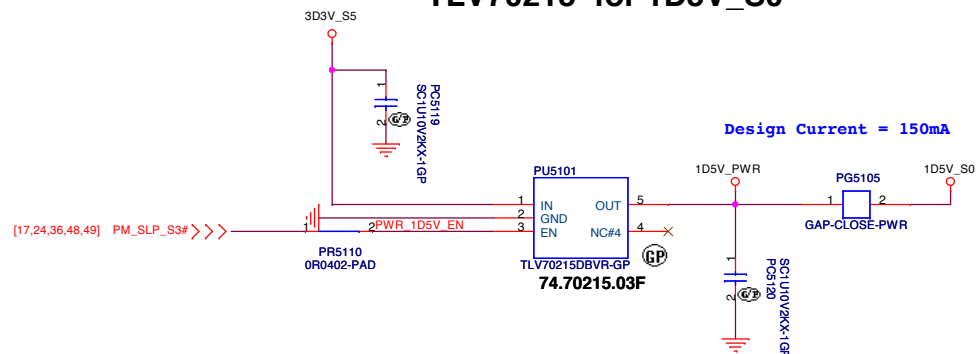
Reserved

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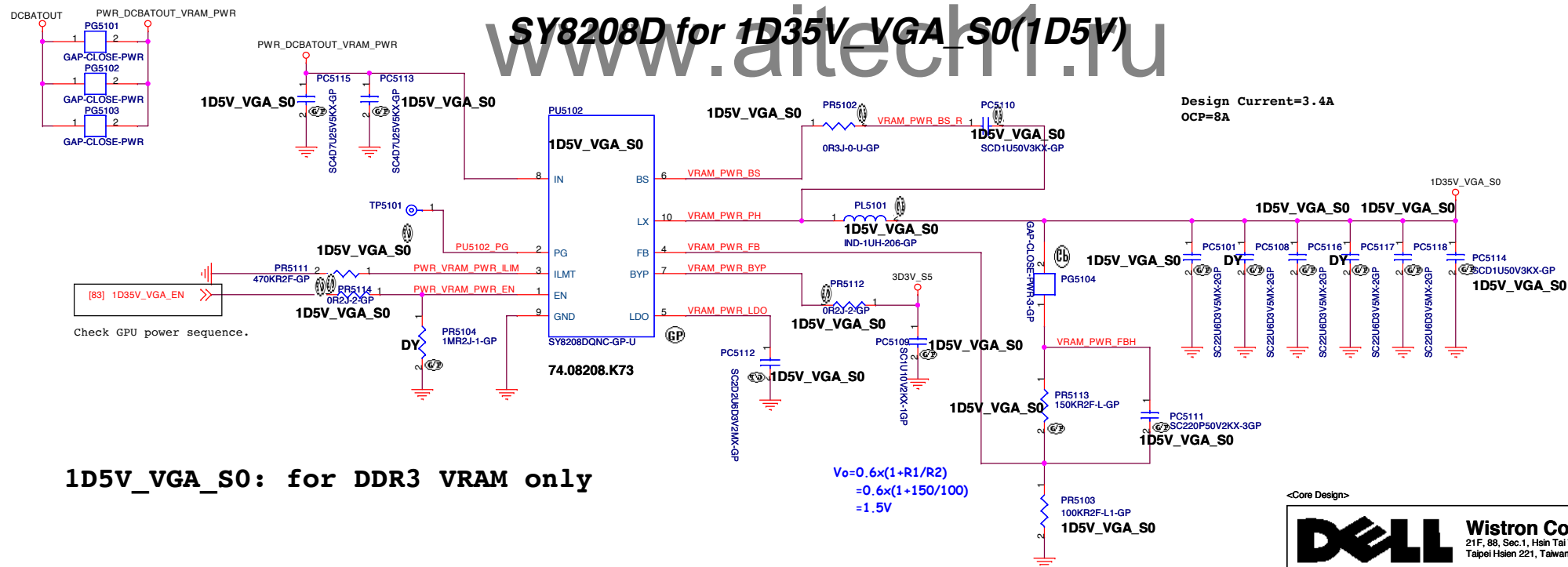
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---------------------------------	-----------------

```
SSID = PWR.Plane.Regulator_1p5v
```

TLV70215 for 1D5V_S0



SY8208D for 1D35V_VGA_S0(1D5V)



1D5V VGA S0: for DDR3 VRAM only

$$\begin{aligned} V_o &= 0.6 \times (1 + R_1/R_2) \\ &= 0.6 \times (1 + 150/100) \\ &= 1.5V \end{aligned}$$

<Core Design>

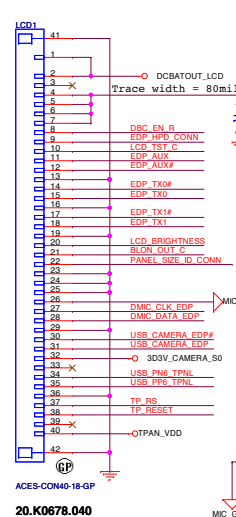


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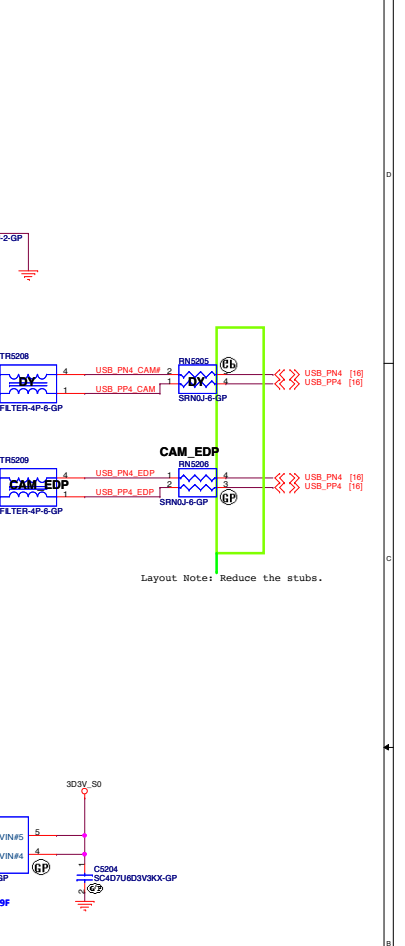
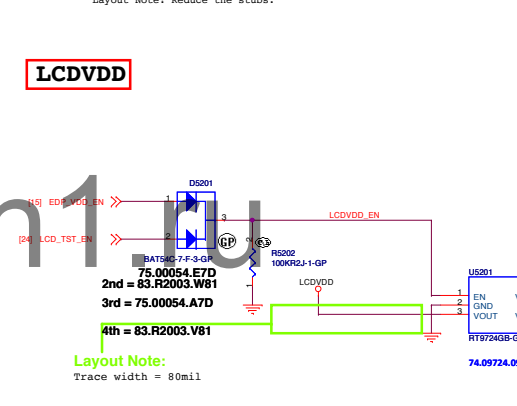
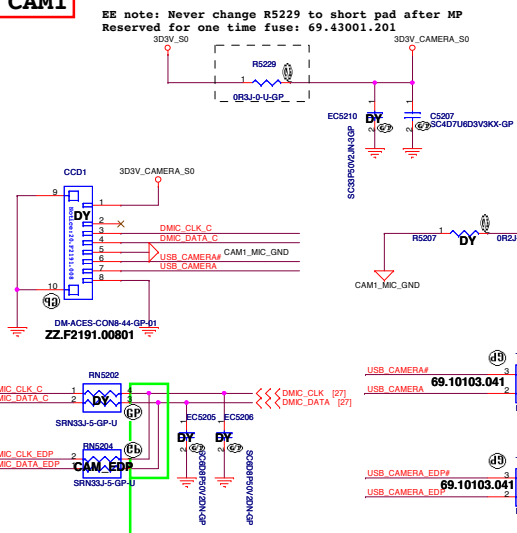
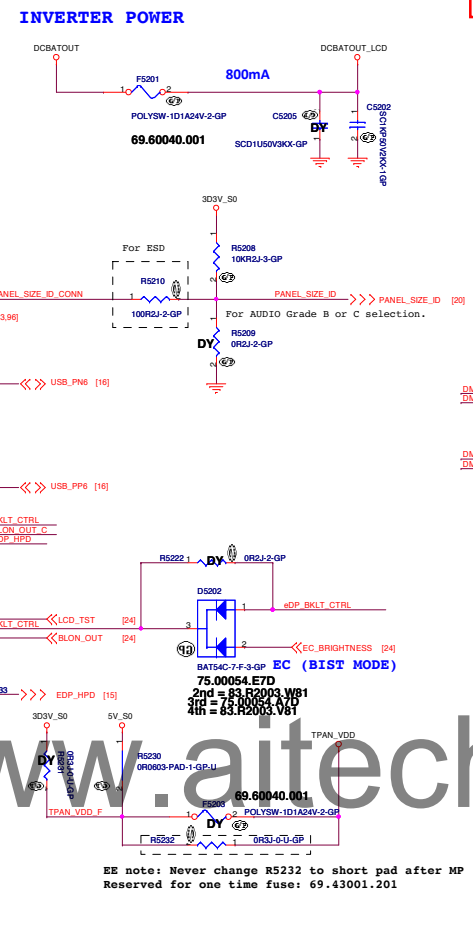
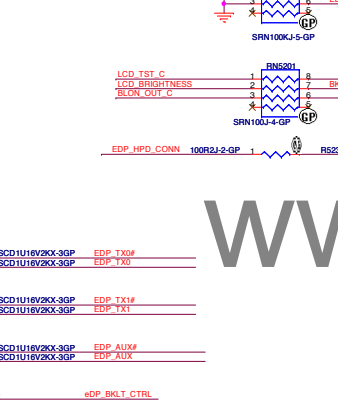
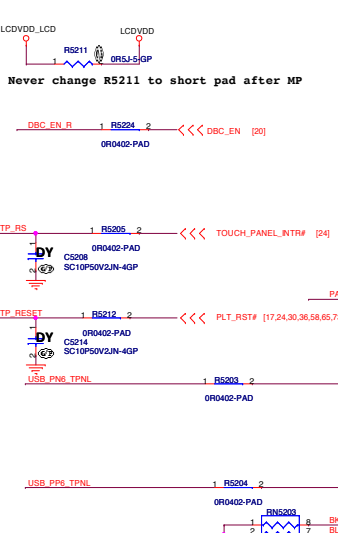
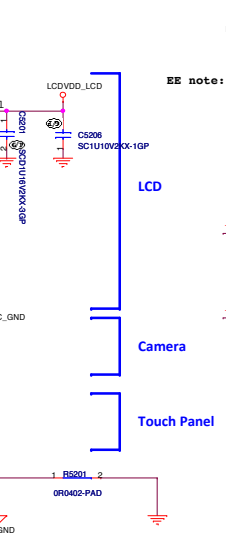
Title
TLV70215 1D5V / SY8208D 1D5V(VGA)

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LCD_BRIGHTNESS	1	AFTPS203
LCD_TST_C	1	AFTPS205
LCD_TST_C	1	AFTPS207
EDP_TX0#	1	AFTPS206
EDP_TX0#	1	AFTPS208
EDP_TX0#	1	AFTPS213
EDP_TX0#	1	AFTPS210
EDP_TX1#	1	AFTPS211
EDP_TX1#	1	AFTPS212
DMIC_CLK_C	1	AFTPS222
DMIC_DATA_C	1	AFTPS228
DMIC_DATA_C	1	AFTPS225
DMIC_DATA_C	1	AFTPS226
DMIC_DATA_C	1	AFTPS227
DMIC_DATA_C	1	AFTPS201
DMIC_DATA_C	1	AFTPS202
DMIC_DATA_C	1	AFTPS204
DMIC_DATA_C	1	AFTPS209
DMIC_DATA_C	1	AFTPS214



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Taipei Hsien 221, Taiwan, R.O.C.

Title

HDMI Level Shifter/Connector

Size

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Sheet

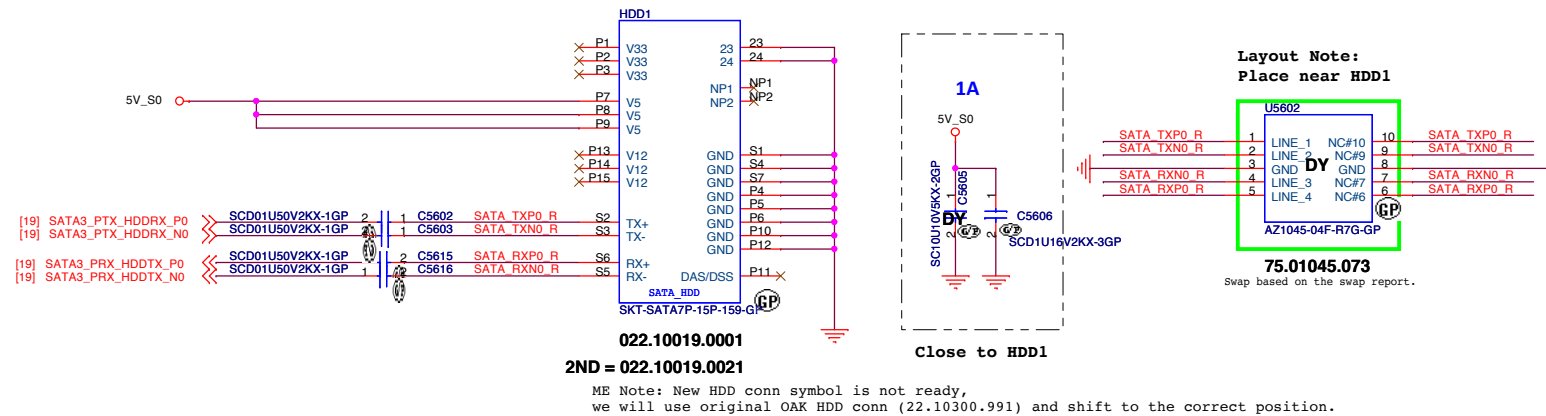
54

 of

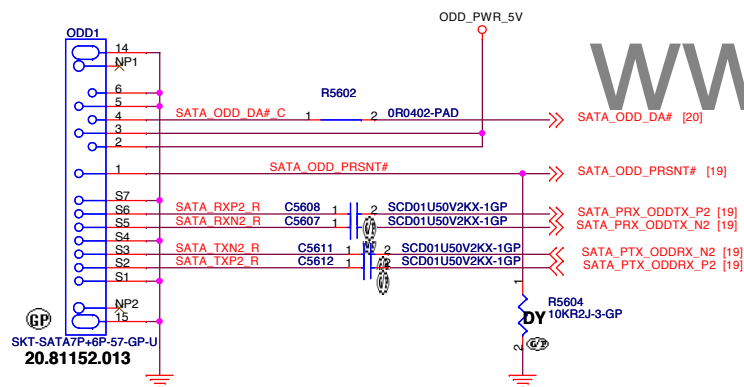
104

SSID = SATA

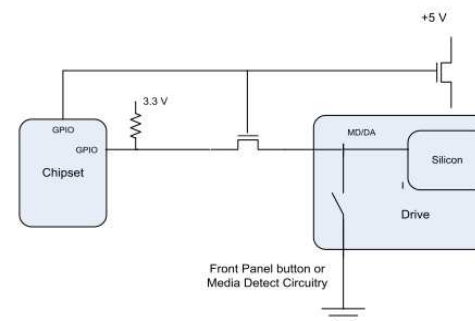
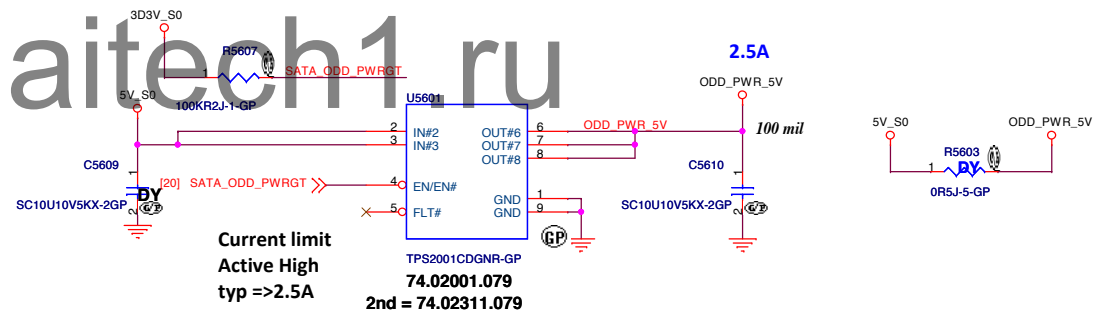
SATA HDD Connector



ODD Connector



SATA Zero Power ODD




<Core Design>

SSID = ESATA

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Title

ESATA

Size
A3

Document Number
Janus HSW 40/50/70

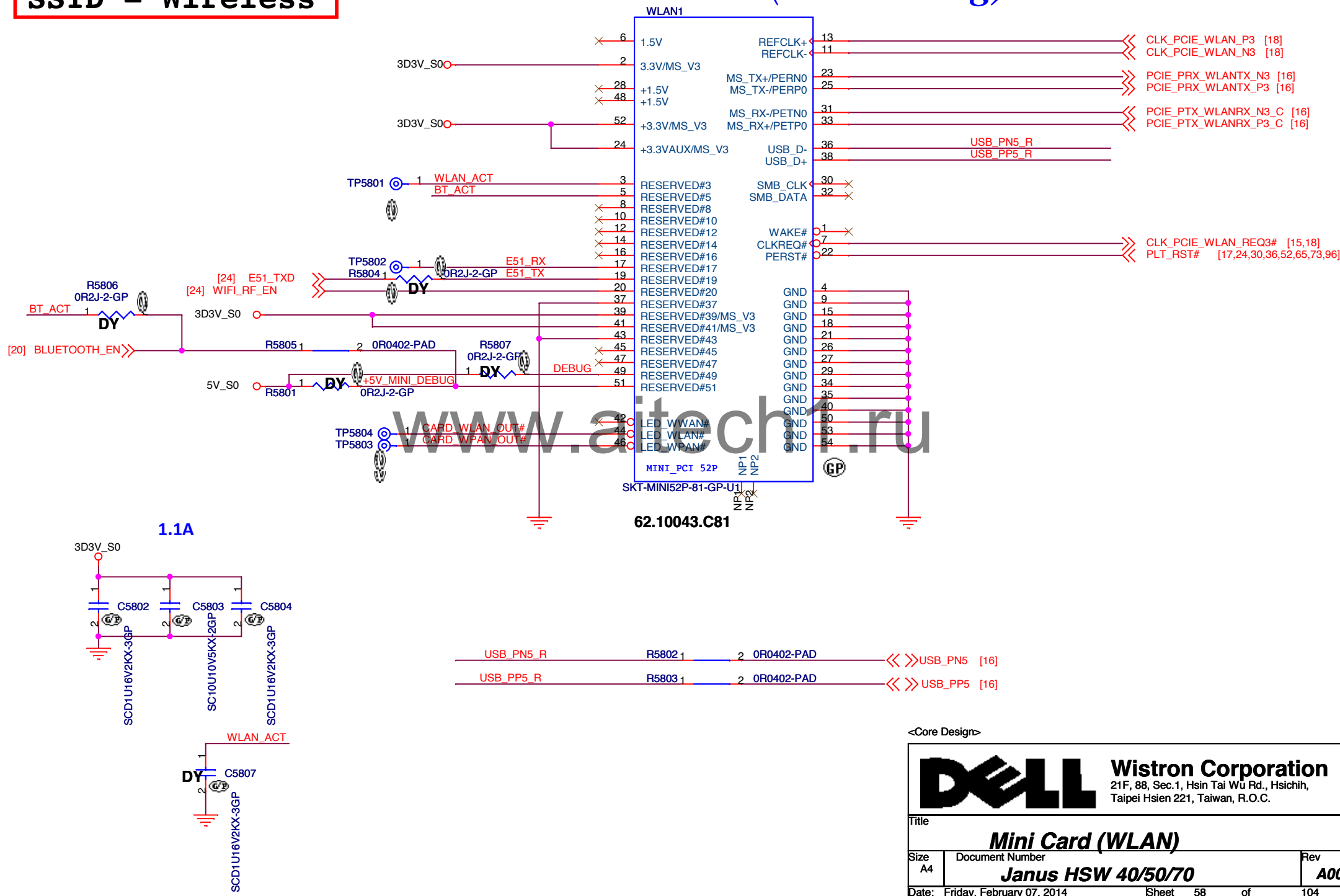
Date: Friday, February 07, 2014

Rev
A00

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SSID = Wireless

Mini Card Connector(802.11a/b/g)



<Core Design>



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Title

Mini Card (WLAN)

Size

A4

Document Number

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Rev

A00

Date: Friday, February 07, 2014

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Title			
Reserved			
Size A4	Document Number Janus HSW 40/50/70		Rev A00
Date: Friday, February 07, 2014		Sheet 59 of	104

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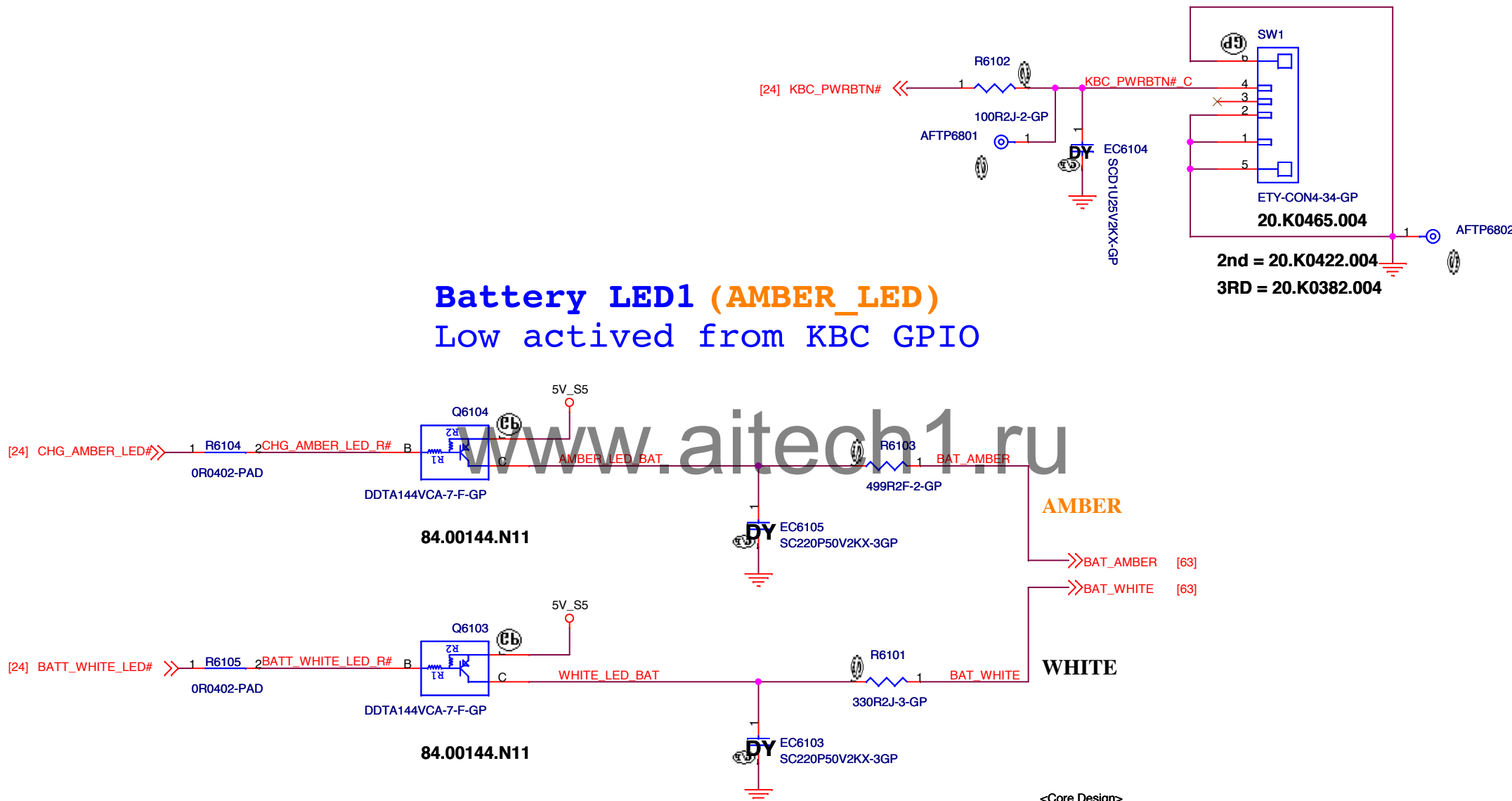
<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
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SSID = User.Interface

Power button

Battery LED1 (AMBER_LED)
Low actived from KBC GPIO



Battery LED2 (WHITE_LED)
Low actived from KBC GPIO

<Core Design>

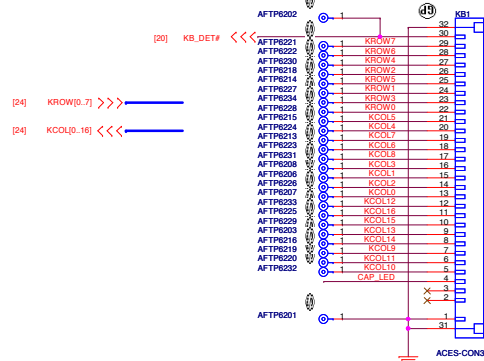


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Title			LED Bard/Power Button	
Size	Document Number		Rev	
A4	Janus HSW 40/50/70		A00	
Date:	Friday, February 07, 2014		Sheet	61 of 104

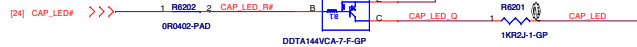
SSID = KBC

Internal Keyboard Connector (DVC40)



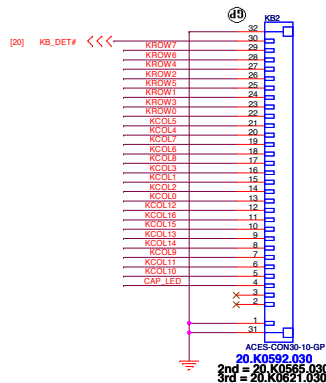
20.K0592.030
2nd = 20.K0565.030
3rd = 20.K0621.030

CAP LED Control
LOW actived from KBC GPIO

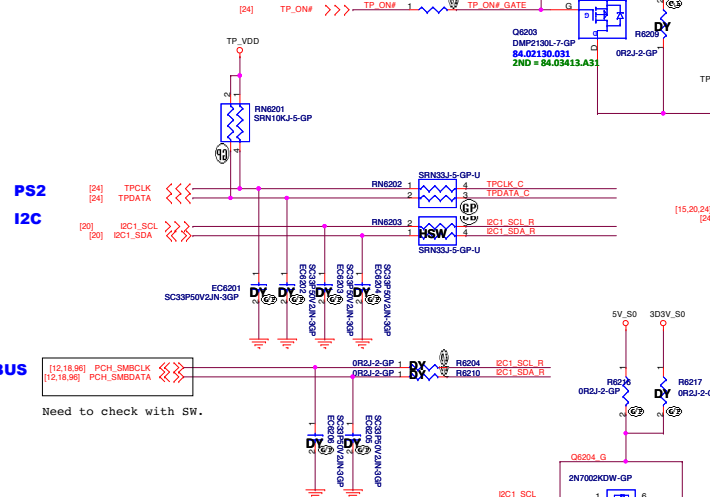


84.00144.N11

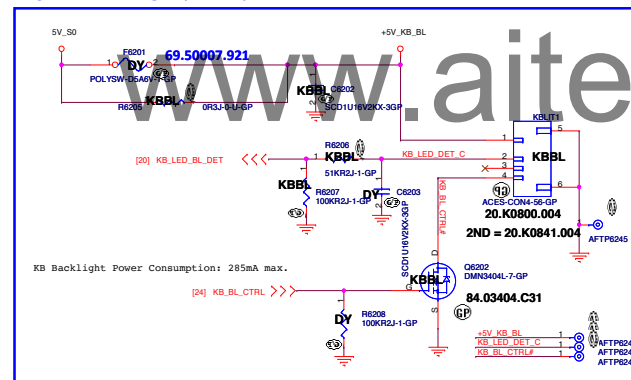
Internal Keyboard Connector (DVC50/DVC70)



20.K0592.030
2nd = 20.K0565.030
3rd = 20.K0621.030

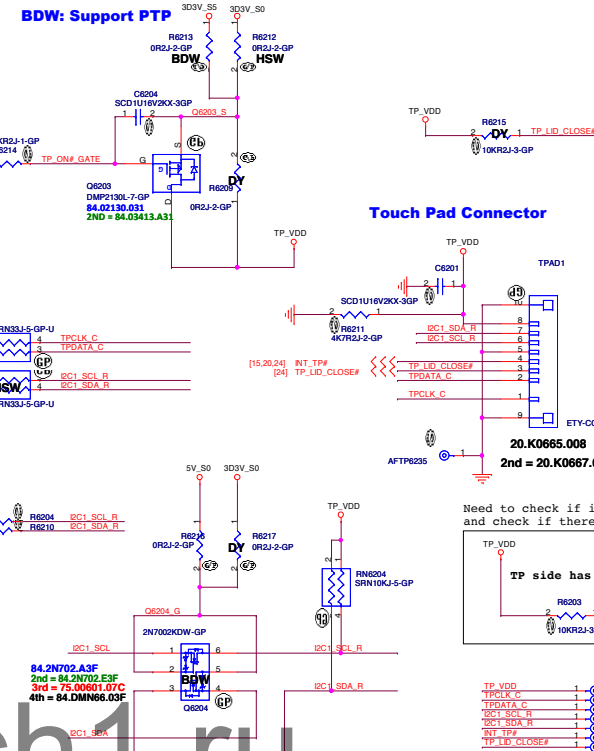
SSID = Touch.Pad

Keyboard Backlight (DVC70)



KB Backlight Power Consumption: 285mA max.

BDW: Support PTP 3D3V_S5 3D3V_S0



Touch Pad Connector

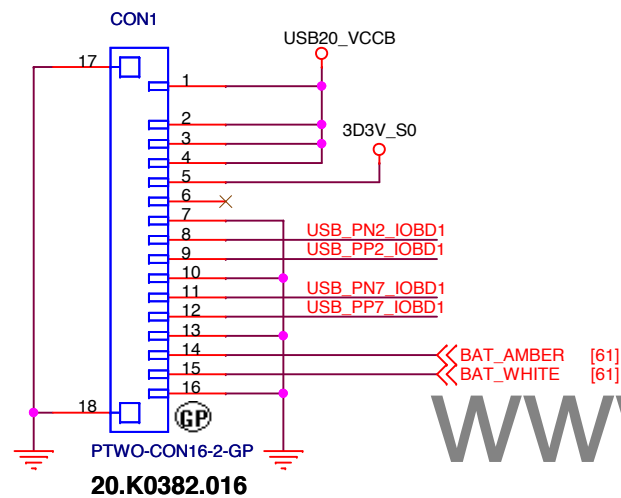
Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(PS2)
8	CLK(PS2)

20.K0665.008
2nd = 20.K0667.008

Need to check if it is Active High or Active Low
and check if there is PH on TPAD side.

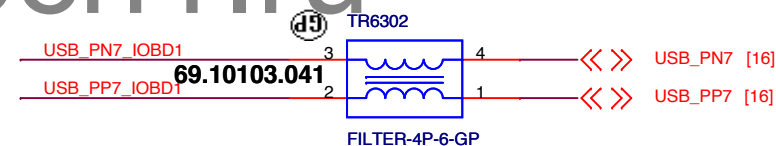
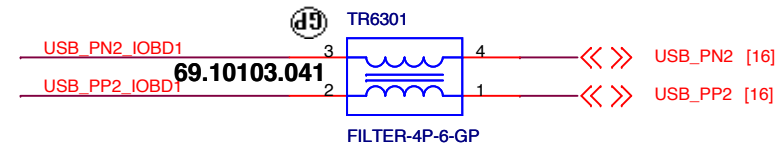
TP side has pull high

TP_VDD	1	AFTP623
TPCLK_C	1	AFTP623
TPDATA_C	1	AFTP623
E2C1_SCL_R	1	AFTP623
E2C1_SDA_R	1	AFTP624
INT_TP#	1	AFTP624
TP_LID_CLOSE#	1	AFTP624

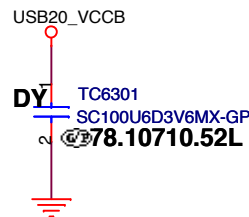


USB2.0 Port3 **Card Reader** **LED**

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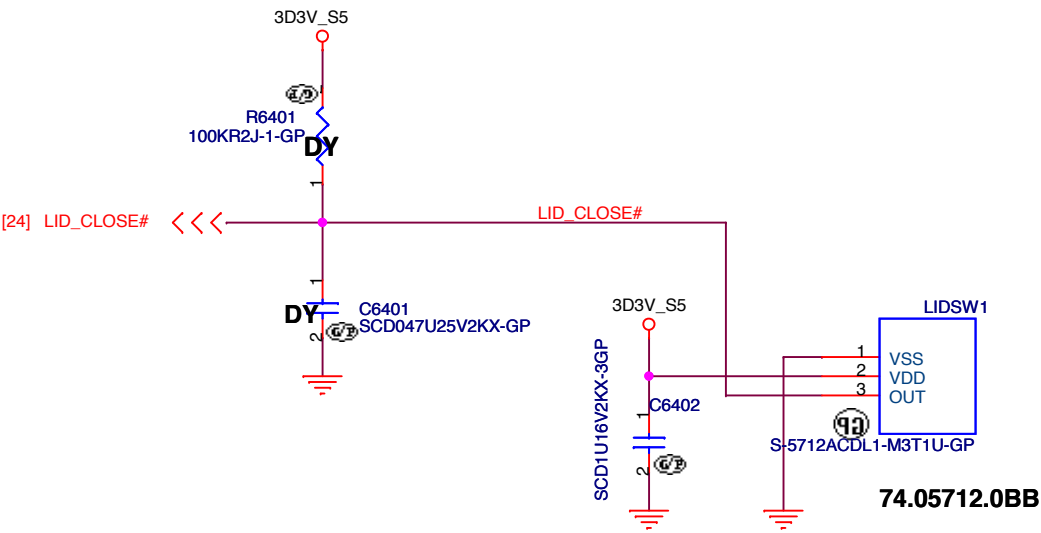
The maximum range of the PMOS output current in RTS5170 (Card Reader IC) is 400mA



<Core Design>


		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		Title IO Board Connector	
Size A4	Document Number Janus HSW 40/50/70		Rev A00
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SSID = User.Interface

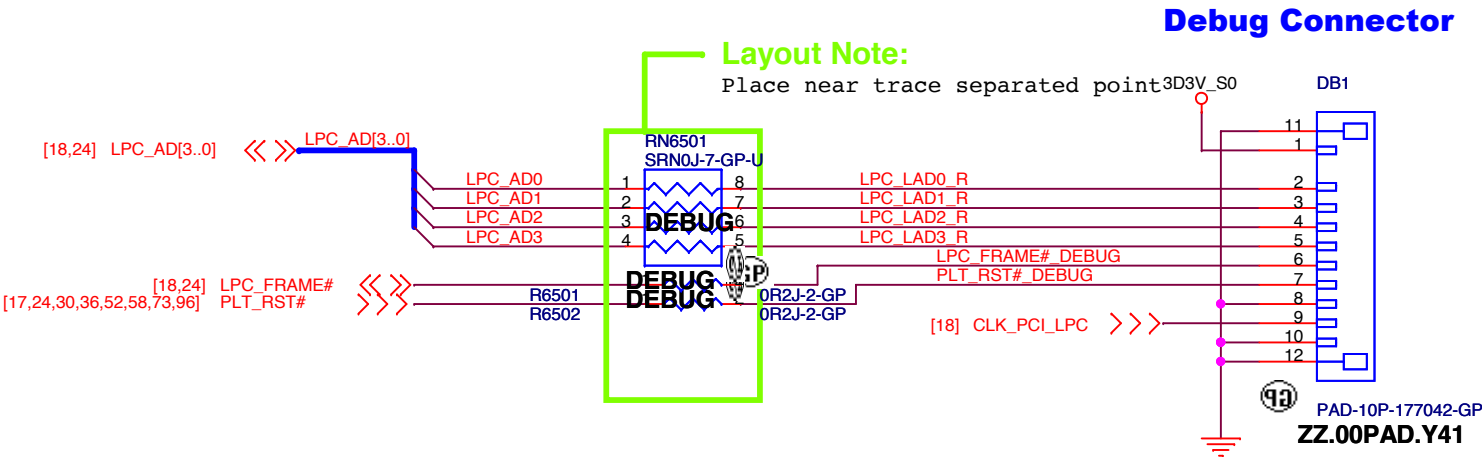


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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Hall Sensor			
Size A4	Document Number Janus HSW 40/50/70		Rev A00
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SSID = DEBUG PORT



20.D0075.110: Dummy Pad with solder mask is ZZ.00PAD.Y41
DB1 Optional: New one smaller LPC connector is 20.F1180.010.

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Title

Dubug connector

Size A4	Document Number Janus HSW 40/50/70	Rev A00
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Reserved			
Size A4	Document Number Janus HSW 40/50/70		Rev A00
Date: Friday, February 07, 2014		Sheet 66 of	104

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Title

Reserved

Size A3	Document Number Janus HSW 40/50/70	Rev A00
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Title			RESERVED	
Size	Document Number	Rev		
A3	Janus HSW 40/50/70	A00		
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Title

USB3.0 PORT

Size
A3

Document Number
Janus HSW 40/50/70

Rev
A00


Date: Friday, February 07, 2014

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A3

Document Number
Janus HSW 40/50/70

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Title

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Size A3	Document Number Janus HSW 40/50/70	Rev A00
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Title

Size
A3

Document Number
Janus HSW 40/50/70

Date: Friday, February 07, 2014

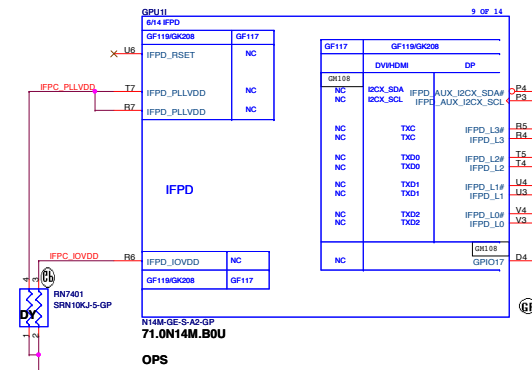
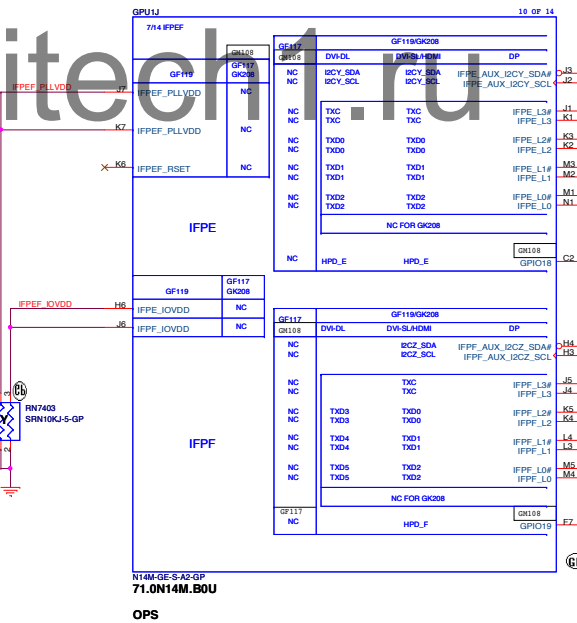
Reserved

Rev
A00

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1

GPU1G		7 OF 14	
414 IFPB		GI108	GI118
GI108		GF117	GF118G208
GF118G208	GF117	NC	IFPA, TXC4 IFPA, TXC
IFPB, RSET	NC	NC	IFPA, TXD0F IFPA, TXD0
IFPB, PLLVDD	NC	NC	IFPA, TXD1F IFPA, TXD1
IFPB, PLLVDD	NC	NC	IFPA, TXD2F IFPA, TXD2
		NC	IFPA, TXD3F IFPA, TXD3
		NC	IFPB, TXC4 IFPB, TXC
		NC	IFPB, TXD4F IFPB, TXD4
		NC	IFPB, TXD5F IFPB, TXD5
		NC	IFPB, TXD6F IFPB, TXD6
		NC	IFPB, TXD7F IFPB, TXD7
		NC	
		GI118	GI118
		GI118	GI118

[illegible]

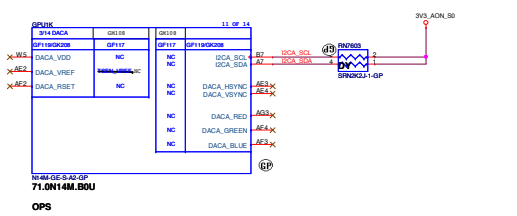


Table 3-32. GB2B-64 and GB4B-128 PLLVDD Filtering

GPU Package	PLL Rail	Capacitor Type	Footprint	Population	Location
GB2B-64 and GB4B-128	PLLVDD	0.1 μ F	X7R	0402	Under GPU
		22 μ F	X5R	0805	Near GPU
		Bead Type			
		30 Ω (ESR=0.05)	0402	1	Near GPU

Table 3-33. SP_PLLVDD and VID_PLLVDD Power Rail Filtering Combined

GPU Package	PLL Rails	Capacitor Type	Footprint	Population	Location
GB2B-64	SP_PLLVDD + VID_PLLVDD	0.1 μ F	X7R	0402	Under GPU
GB4B-128		4.7 μ F	X5R	0603	Near GPU
GB3-256		22 μ F	X5R	0805	Near GPU
		Bead Type			
		180 Ω (ESR=0.2)	0603	1	Near GPU

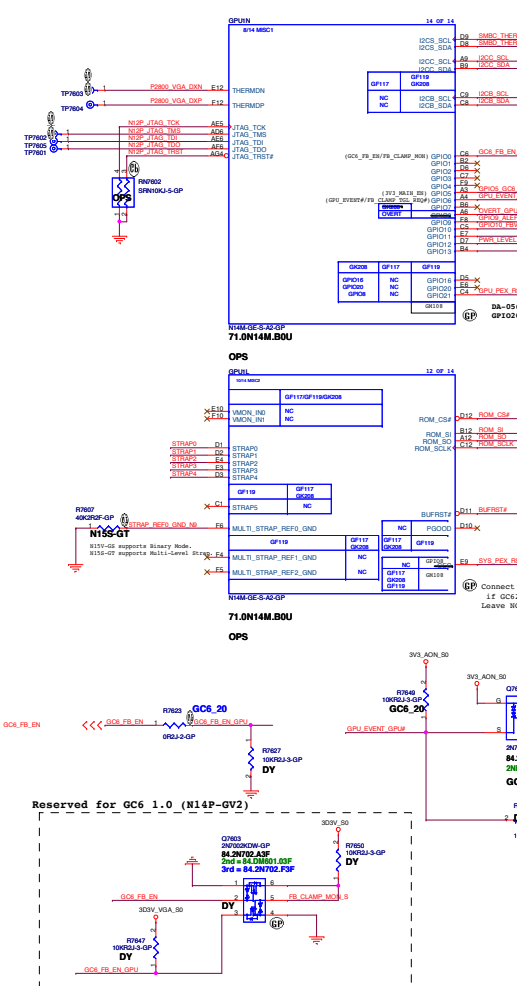


Table 3-34. GB2B-64 and GB4B-128 Power Rail Filtering Combined

GPU Package	Power Rail	Capacitor Type	Footprint	Population	Location
GB2B-64 and GB4B-128	Power Rail	0.1 μ F	X7R	0402	Under GPU
		22 μ F	X5R	0805	Near GPU
		Bead Type			
		180 Ω (ESR=0.2)	0603	1	Near GPU

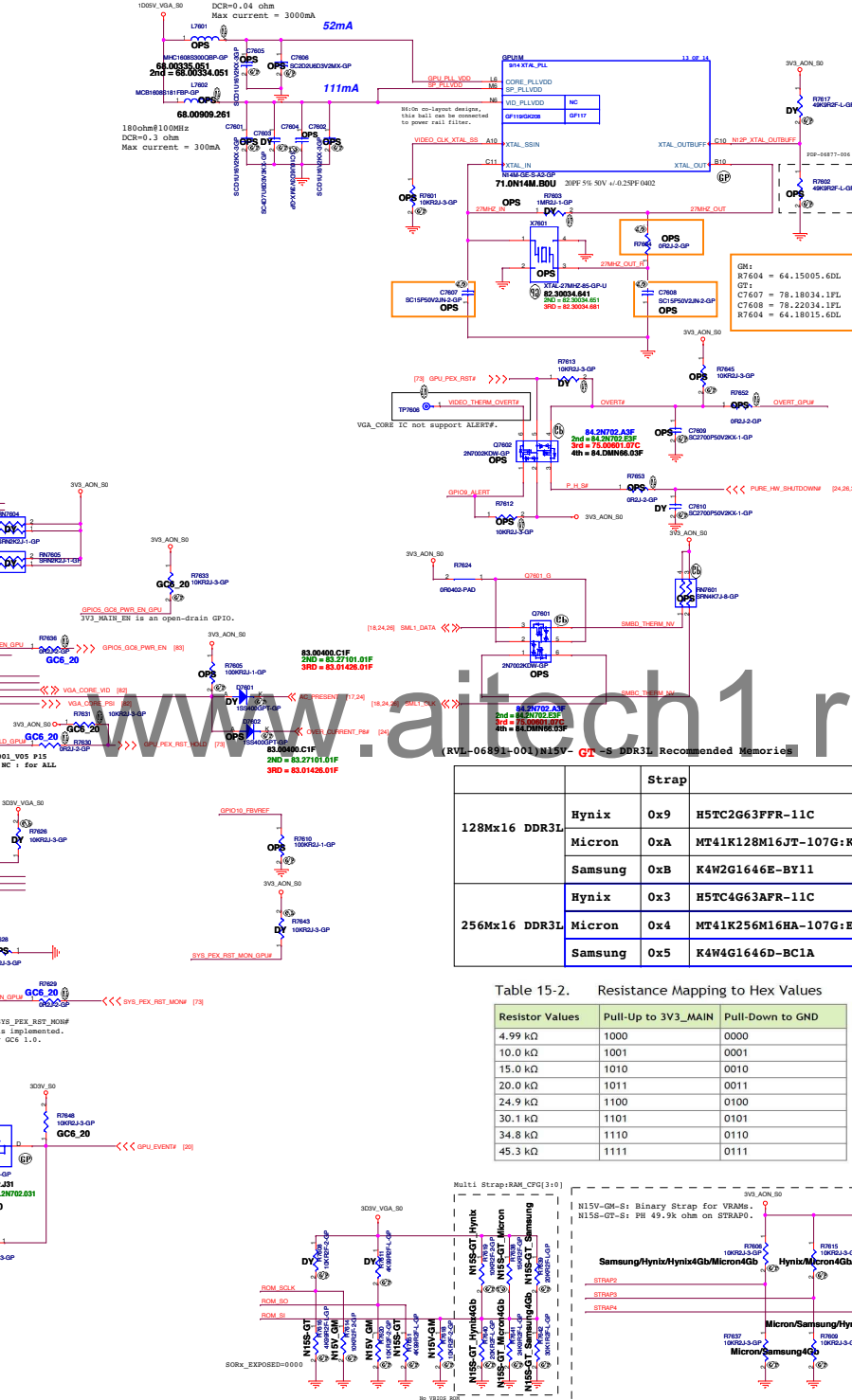


Table 3-35. GB2B-64 and GB4B-128 Power Rail Filtering Combined

GPU Package	Power Rail	Capacitor Type	Footprint	Population	Location
GB2B-64 and GB4B-128	Power Rail	0.1 μ F	X7R	0402	Under GPU
		22 μ F	X5R	0805	Near GPU
		Bead Type			
		180 Ω (ESR=0.2)	0603	1	Near GPU

Straps

(DS-06814-001)

Table 9. N15V-GM Binary Strap Mode Mapping

Strap Pin Name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10k Ω	Pull-down to GND
ROM_SI	SUB_VEHODR	10k Ω	+Pull-up to 3V3 if VBIOS ROM exists +Pull-down to GND if no VBIOS ROM
ROM_SO	VGA_DEVICE	10k Ω	Pull-down to GND (no display)
STRAP0	RAM_CFG[0]	10k Ω	See note below
STRAP1	RAM_CFG[1]	10k Ω	See note below
STRAP2	RAM_CFG[2]	10k Ω	See note below
STRAP3	RAM_CFG[3]	10k Ω	See note below
STRAP4	PCIE_MAX_SPEED	10k Ω	Pull-down to GND

(RVL-06891-001)N15V- GM-S DDR3L Recommended Memories

		Strap		STRAP3	STRAP2	STRAP1	STRAP0
128Mx16 DDR3L	Hynix	Ox	H5TC2G63FPR-11C	1	1	0	0
	Micron	Ox1	MT41K128M16JT-107G:K	0	0	0	1
	Samsung	Ox5	K4W2G1646E-BY11	0	1	0	1
256Mx16 DDR3L	Hynix	Ox4	H5TC4G63AFR-11C	0	1	0	0
	Micron	Ox	MT41K256M16HA-107G:E	1	1	0	1
	Samsung	Ox9	K4W4G1646D-BC1A	1	0	0	1

(DS-06814-001)

Table 10. Multi-Level Strap Differences

Physical Strapping Pin	GPU	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	H155-GV	PCI_DEV[4]	SUB_VEHODR	PCI_DEV[5]	PEX_PLN_TERM
ROM_SI	H155-GM/-GT	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SO	H155-GV	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	H155-GM/-GT	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	H155-GM/-GT	Reserved (Keep pull-up and pull-down footprints and stuff 50k pull-up)	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)
STRAP2	H155-GM/-GT	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)
STRAP3	H155-GM/-GT	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)
STRAP4	H155-GM/-GT	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)

Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 k Ω	1000	0000
10.0 k Ω	1001	0001
15.0 k Ω	1010	0010
20.0 k Ω	1011	0011
24.9 k Ω	1100	0100
30.1 k Ω	1101	0101
34.8 k Ω	1110	0110
45.3 k Ω	1111	0111

DS-06812

Chip	N15V-GM	N155-GT
Device ID	0x1140	0x1341
Memory interface	sDDR3	sDDR3
Package	595 ball BGA 23x23mm	408 ball BGA 29 x 29 mm

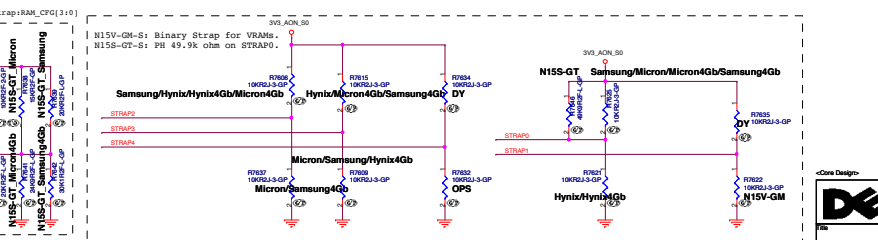
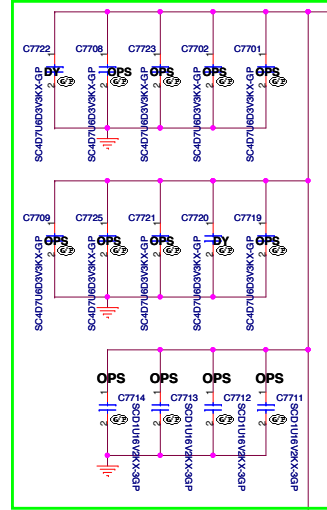


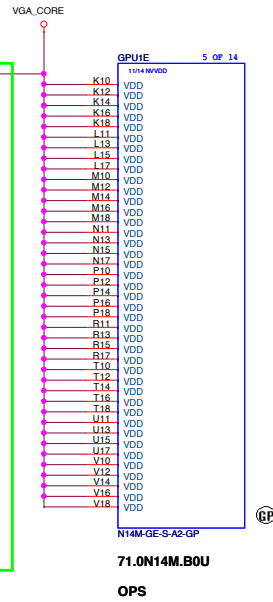
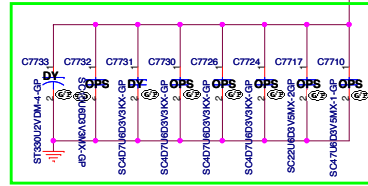
Table 3-36. GB2B-64 and GB4B-128 Power Rail Filtering Combined

GPU Package	Power Rail	Capacitor Type	Footprint	Population	Location
GB2B-64 and GB4B-128	Power Rail	0.1 μ F	X7R	0402	Under GPU
		22 μ F	X5R	0805	Near GPU
		Bead Type			
		180 Ω (ESR=0.2)	0603	1	Near GPU

Under GPU



Near GPU

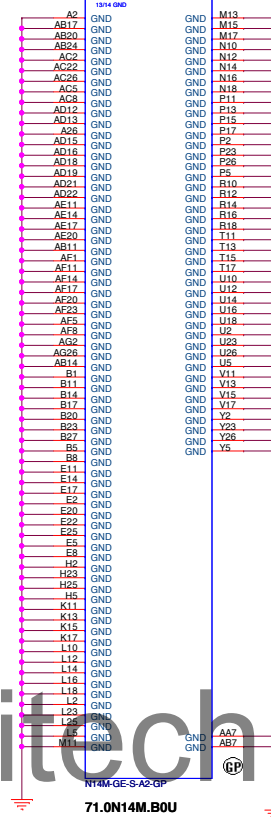


GP

71.0N14M.B0U

OPS

GPU1F 6 OF 14

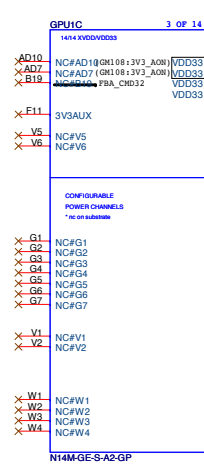


GP

71.0N14M.B0U

OPS

G10,G12:
If GC62.0 is implemented, connect to a 3V3 rail that will be on in GC6.
If GC62.0 is NOT implemented, connect to the same rail as VDD33.



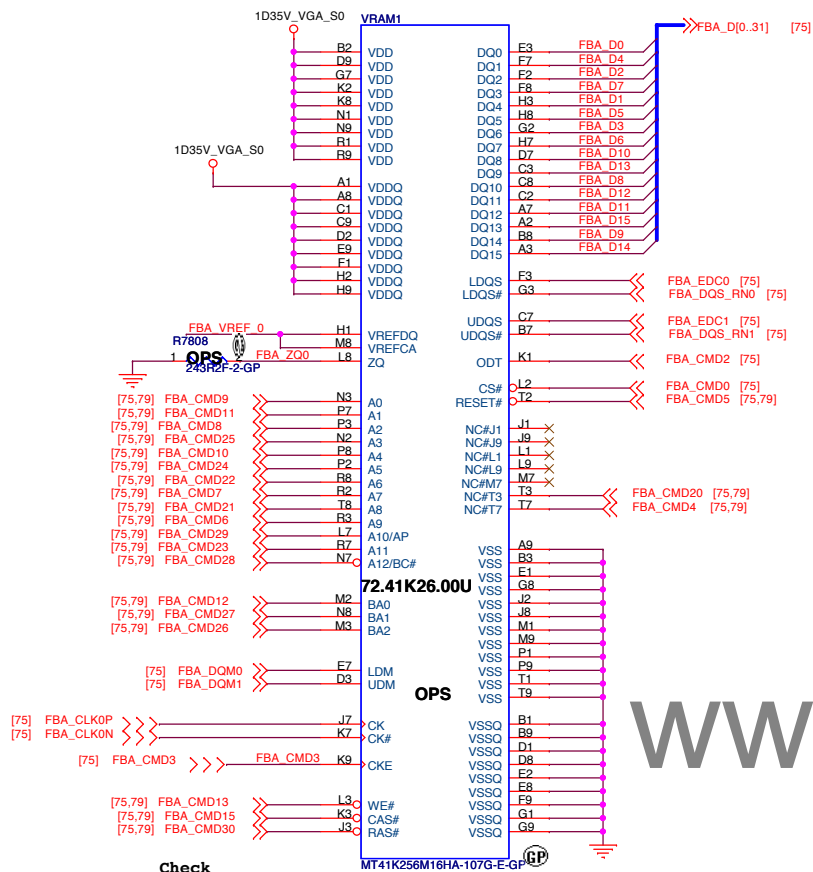
71.0N14M.B0U

OPS

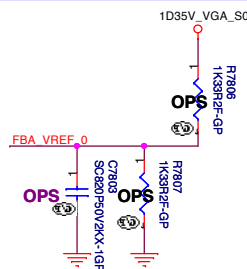
GP

<Core Design>

DELL		Wistron Corporation	
21F, 8B, Sec 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: GPU_DPPWR/GND(5/5)			
Size: Custom	Document Number: Janus HSW 40/50/70	Rev: A00	
Date: Friday, February 07, 2014	Sheet: 77	of	104



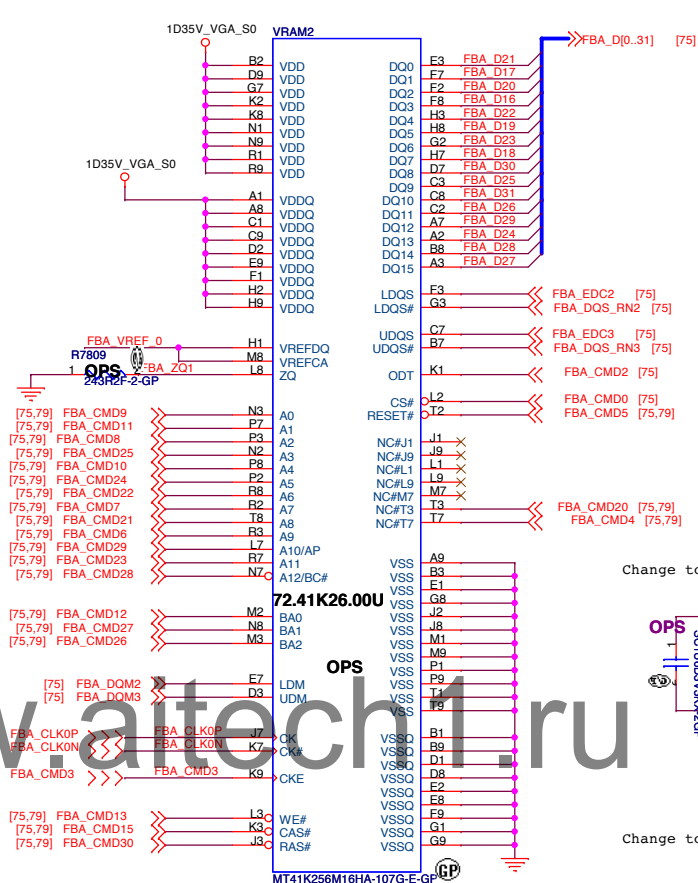
Frame Buffer Partition A-Lower Half



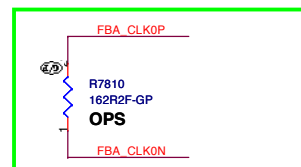
FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low

20110613

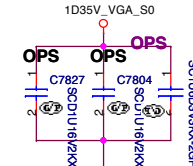


FBCLK Termination place on VRAM side

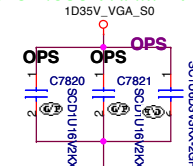


Layout Note: Place in the end.

Place close VRAM1 VDD ball

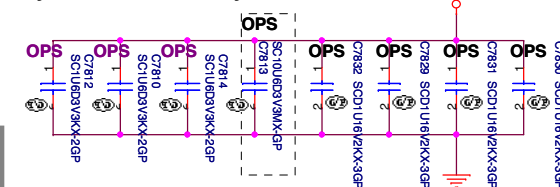


Place close VRAM2 VDD ball



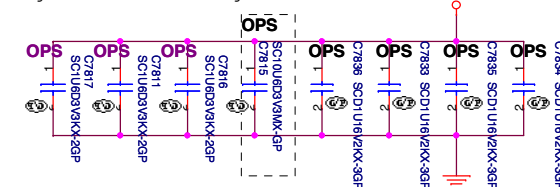
Place close VRAM1VDDQ ball

Change to 10U 0603 for height limit issue.



Place close VRAM1VDDQ ball

Change to 10U 0603 for height limit issue.




<Core Design>

DELL		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: GPU-VRAM1,2 (1/4)			
Size: A3	Document Number:	Rev: A00	
Date: Friday, February 07, 2014		Sheet 78 of 104	

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Title

GPU-VRAM5,6 (3/4)

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GPU-VRAM7,8 (4/4)

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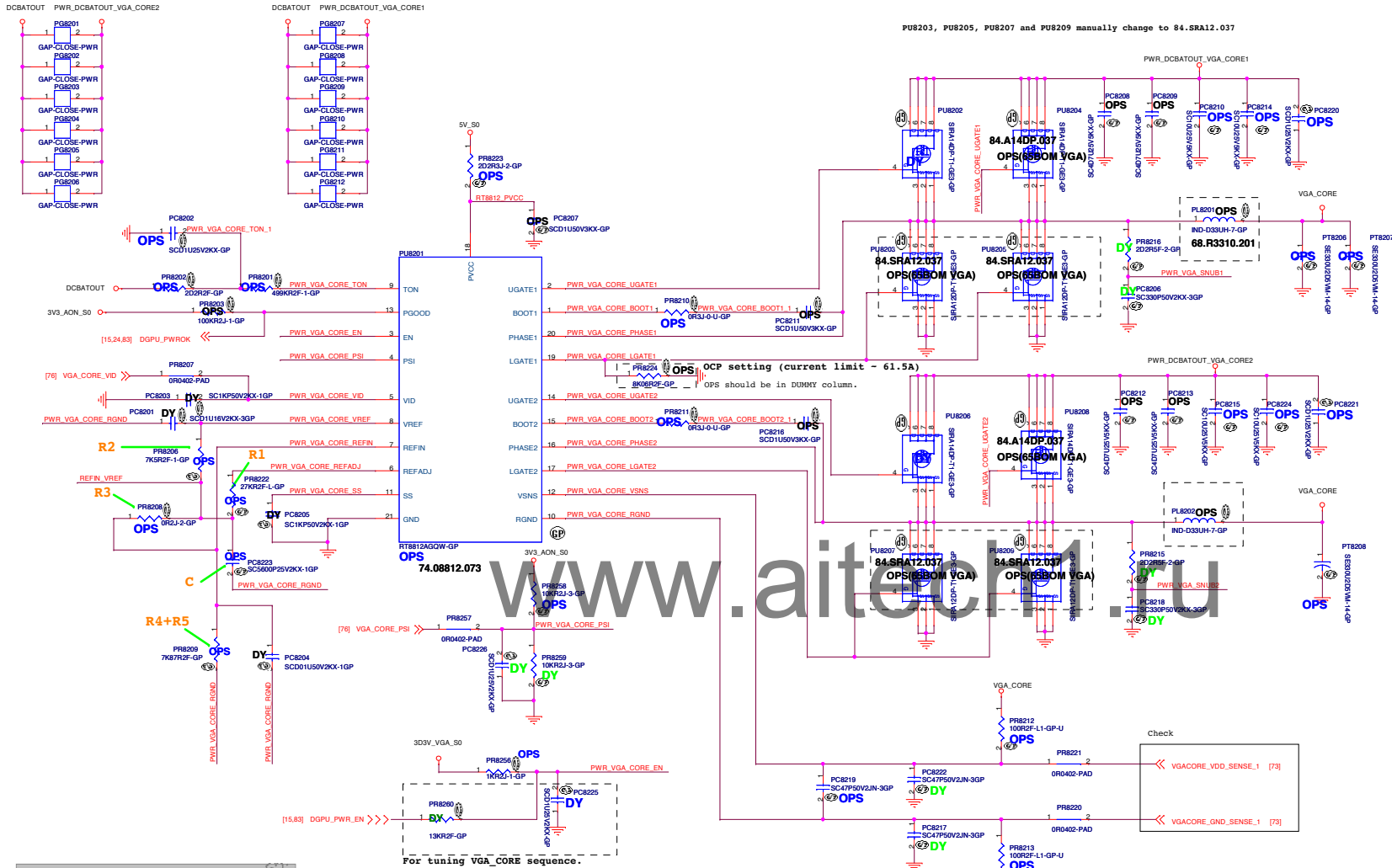
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N15V_GM_S Config D

Design Current=33.5A
56.65A <OCP< 66.7A

Component	N15V-GM-S Config D	N15-S-07-S Config B
R1 (PR8222)	27K 64.27025,60L	20K 64.20025,60L
R2 (PR8206)	7.5K 64.75015,60L	20K 64.20025,60L
R3 (PR8208)	0 63.80034,10L	2K 64.20015,60L
R4+R5 (PR8209)	7.87K 64.78715,60L	18K 64.18025,60L
C (PC8223)	5.6nF 78.56222,2FL	2.7nF 78.27224,2FL


PWM-VID Specification	Config A	Config B	Config C	Config D
Vmin	0.6	0.6	0.6	0.9
Vmax	1.2	1.2	1.15	1.15
Vboot	0.875	0.9	0.9	1.028
Voltage Step Vstep	6.25	6.25	25	12.5
Number of Voltage Levels N	level	96	20	20
PWM Frequency F _{min}	MHz	1.125	0.676	0.676
PWM Minimum Pulse Width T _{min}	μs	9.26	74	74
VID Transient Time T	<100	<100	<100	<100
Component Value				
R1 (1k)	KΩ	39	20	39
R2 (1k)	KΩ	39	20	30
R3 (1k)	KΩ	1.5	2	3
R4 (1k)	KΩ	30	18	24
R5 (1k)	KΩ	1.5	0	3
C	nF	1.5	2.7	1.8

I/P cap: 10U 25V X805 X5R/ 78.10622.51L
Inductor:CHIP CHORE 0.22UH PCMC104T-R22/ 1mohm/ Isat =60A rms /68.R2210.10C
O/P cap: CHIP CAP EL 330U 2.5V M6.3*4.4 Chemi-con/79.3371V.6CL
H/S: SIRA14DP-T1-GE3 / 6.8mohm/8.5mOhm4.5Vgs/ 84.A14DP.037
L/S: SIRA06DP-T1-GE3 / 2.75mohm/3.5mOhm4.5Vgs/ 84.SRA06.037

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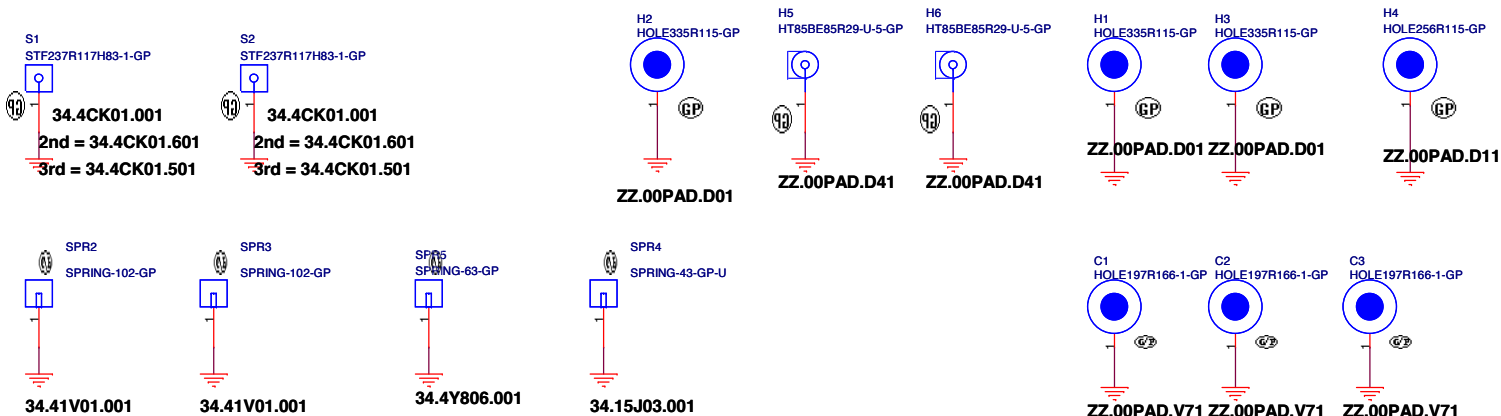
Title

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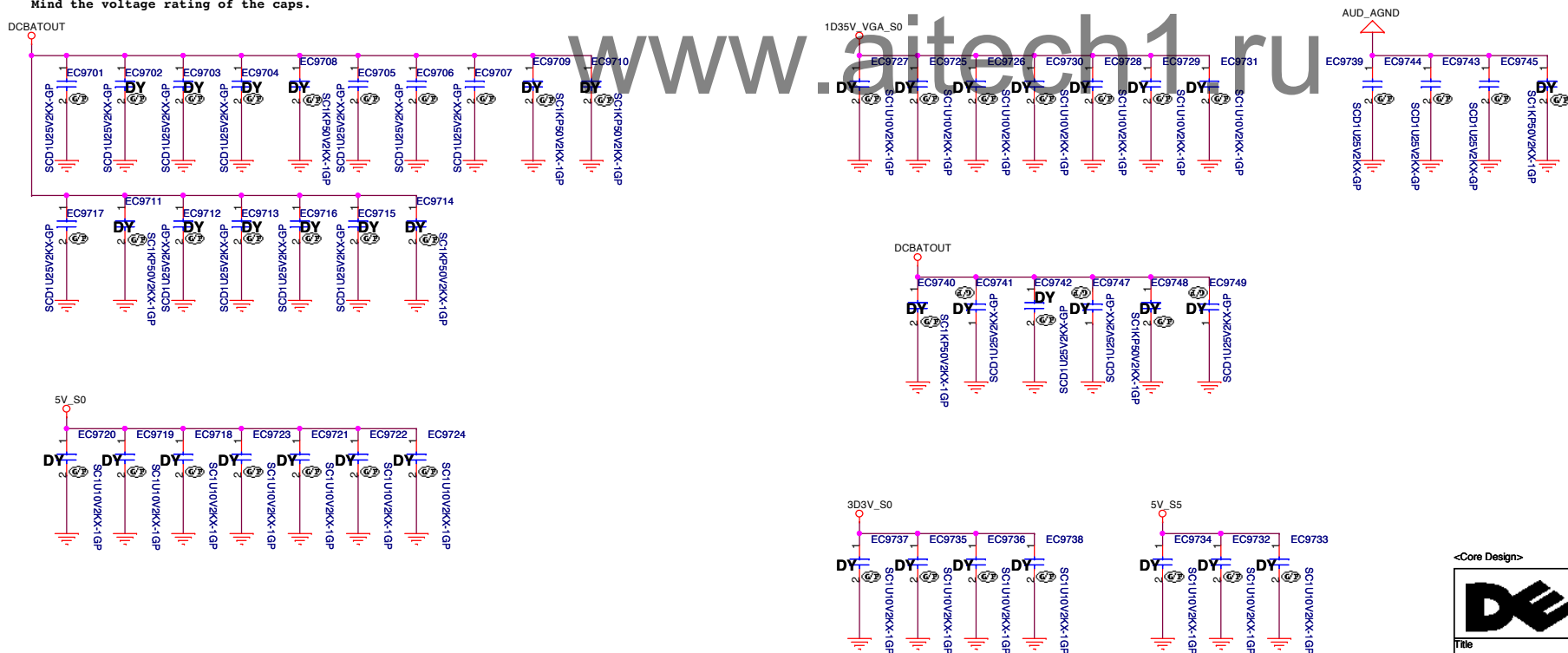
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SSID = Mechanical



SSID = EMI


Mind the voltage rating of the caps.



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Free Fall Sensor


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LVDS Switch

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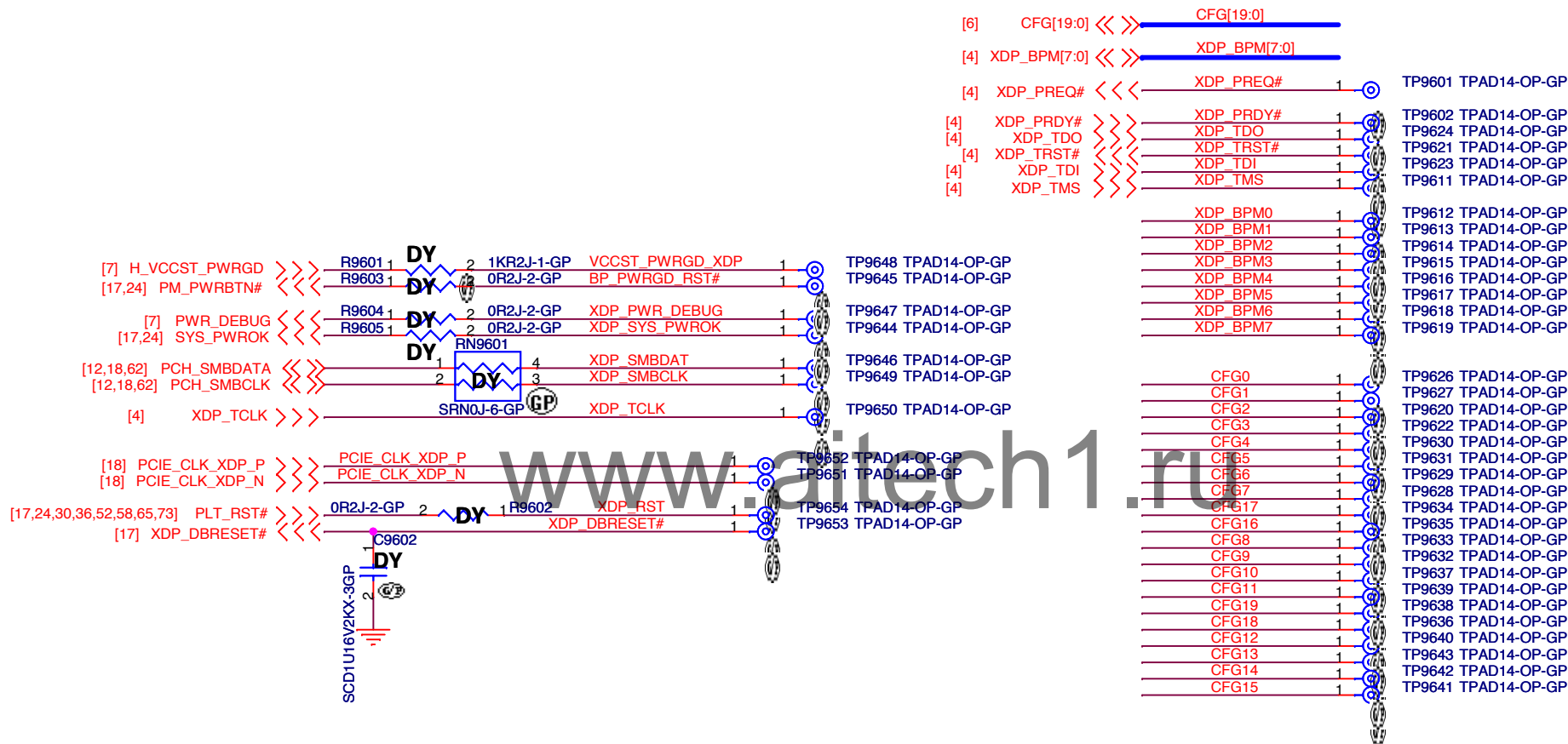
(Blanking)

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SSID = XDP

CPU XDP



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CPU/PCH XDP

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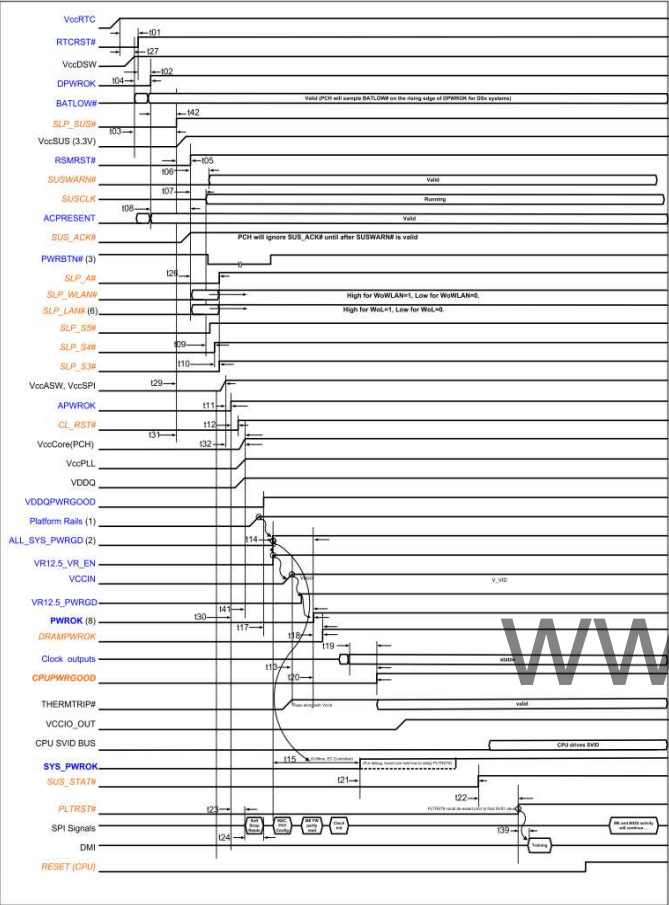
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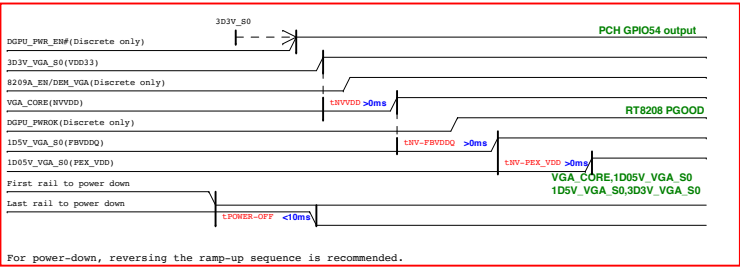
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Shark Bay Platform Power Sequence

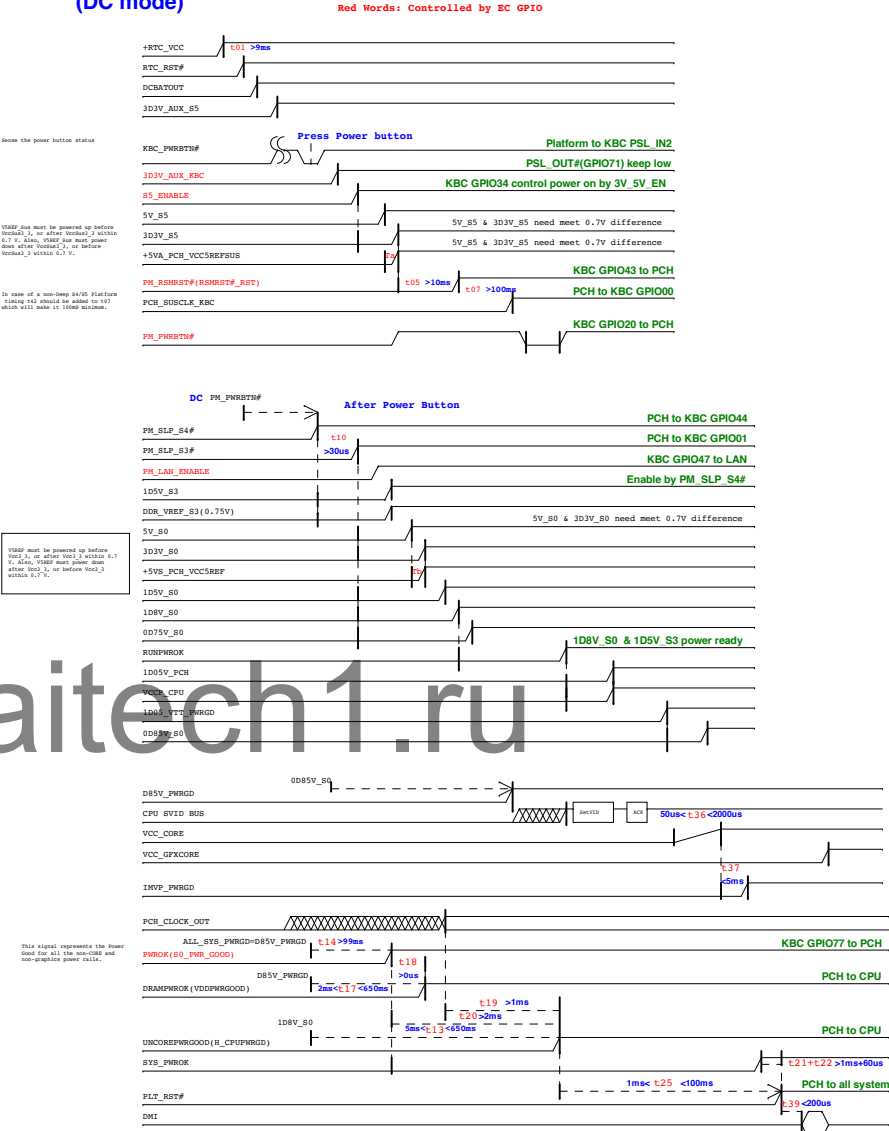


N14P-GT Power-Up/Down Sequence

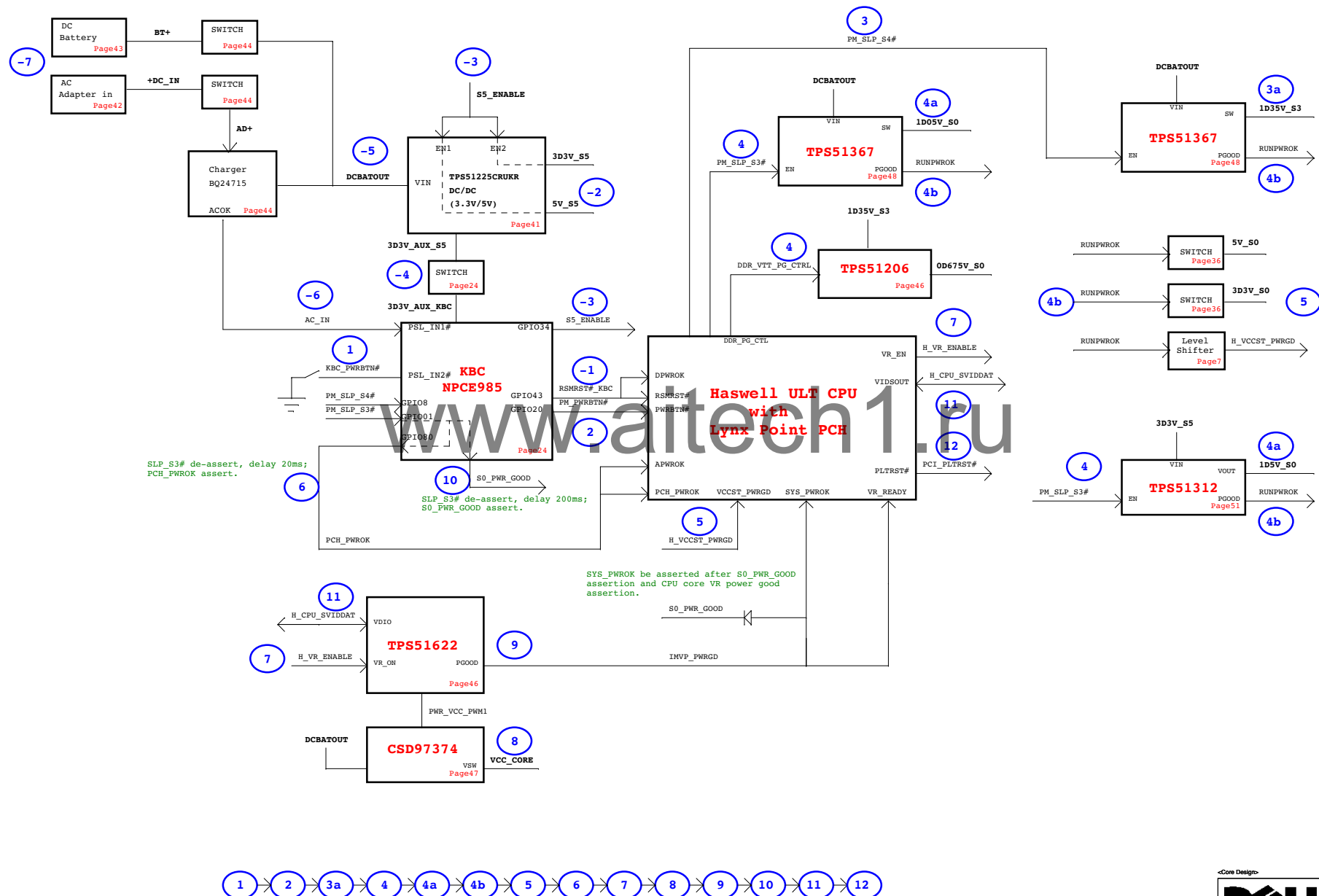


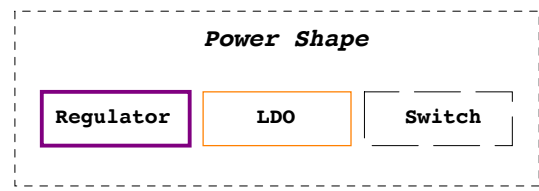
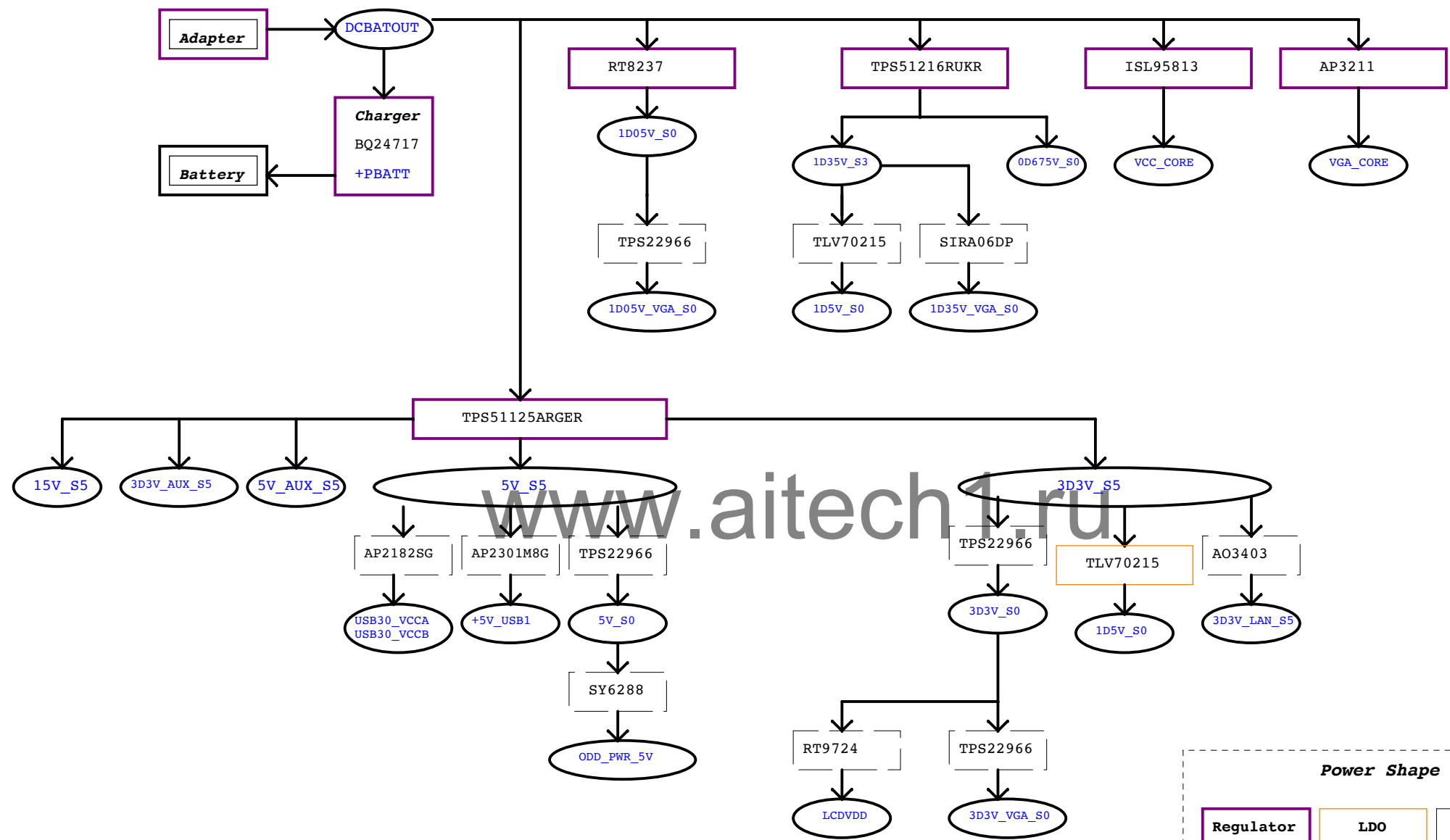
For power-down, reversing the ramp-up sequence is recommended.

(DC mode)

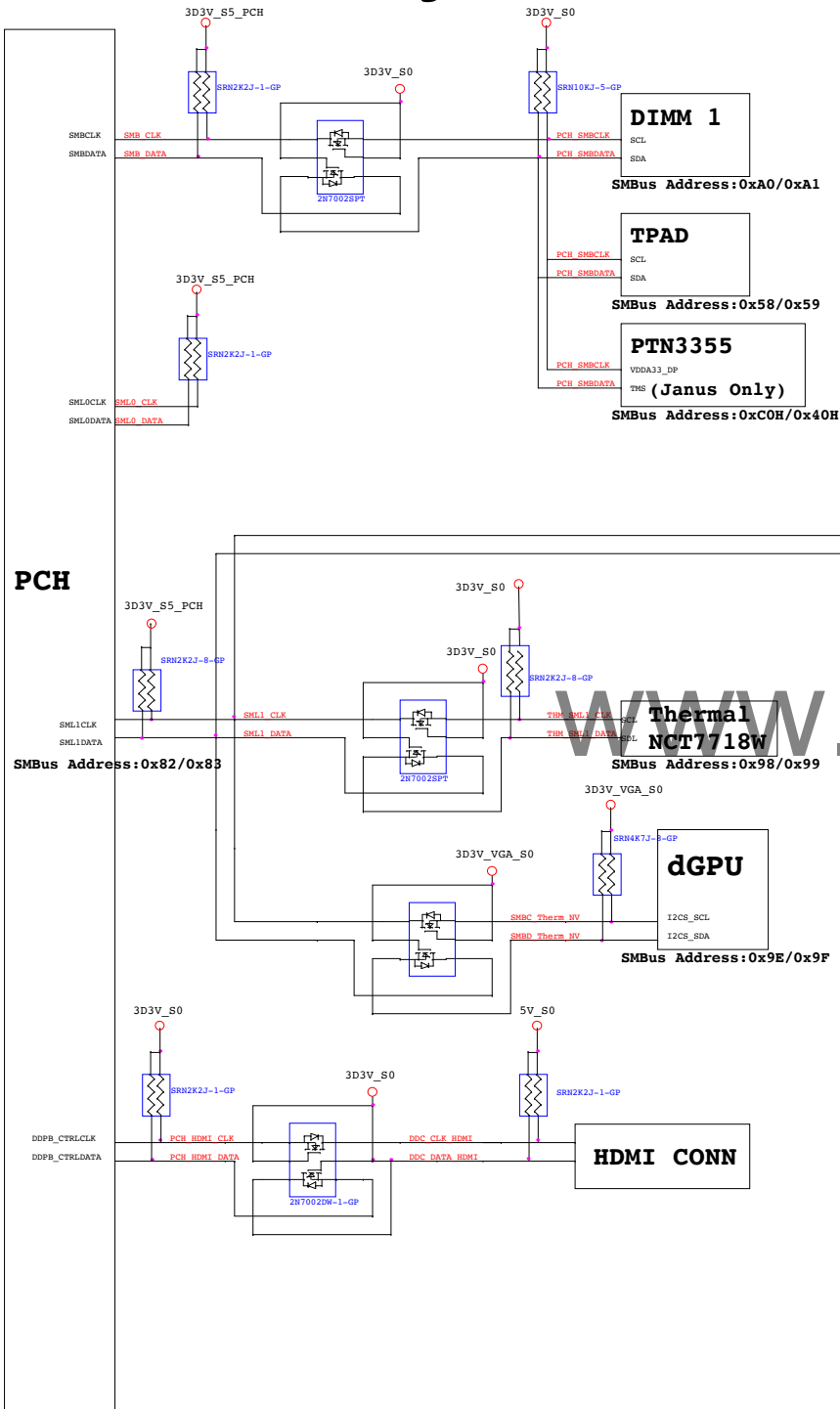


WISTRON SHARK BAY POWER UP SEQUENCE DIAGRAM

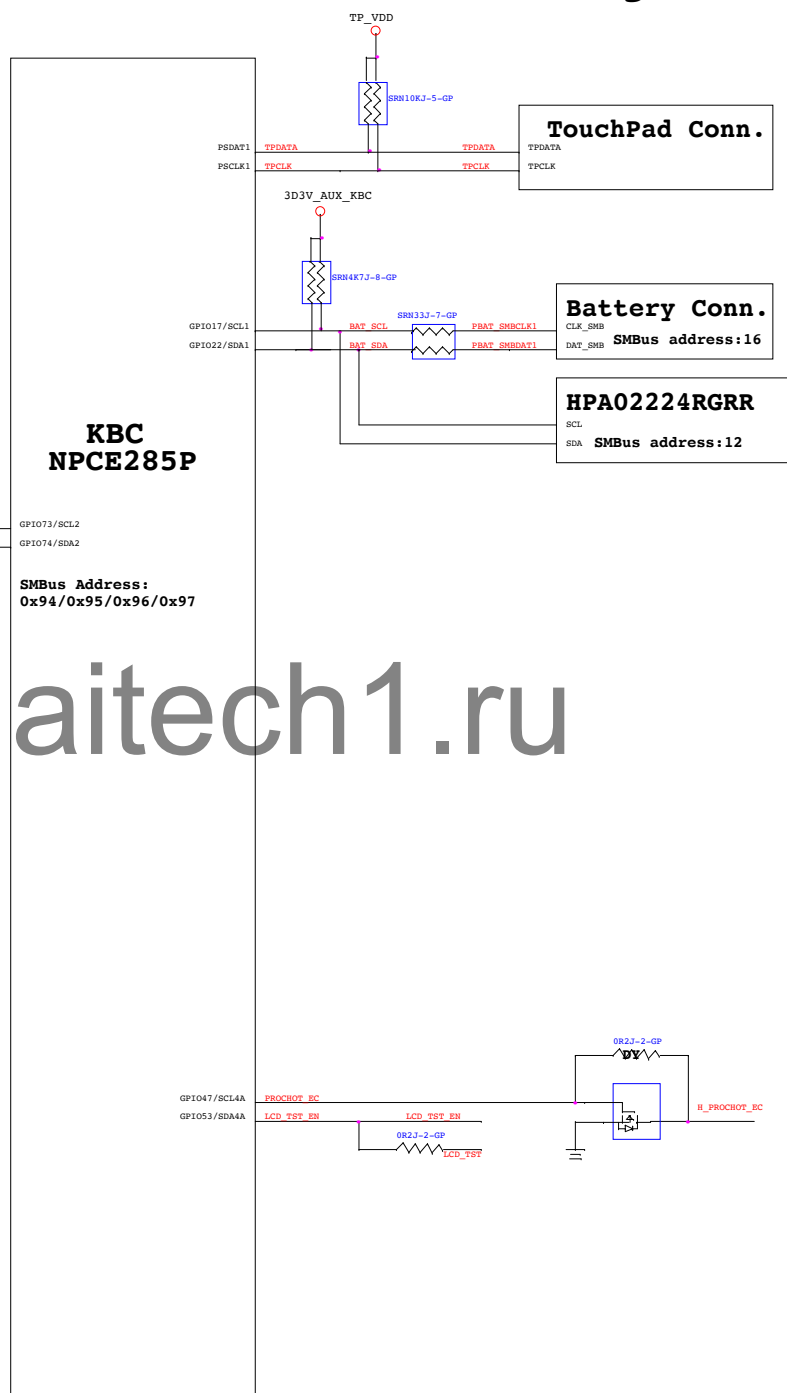




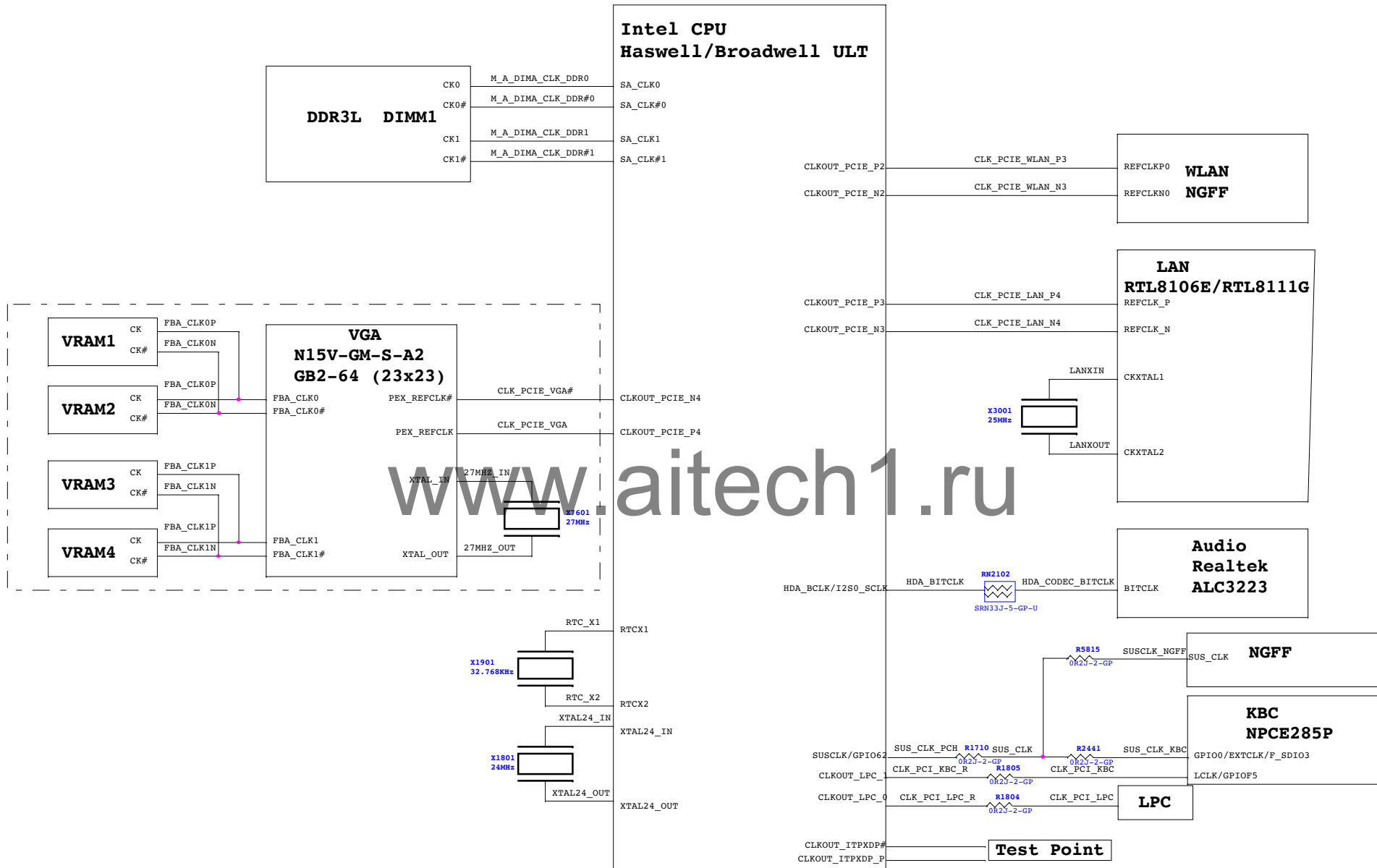
PCH SMBus Block Diagram



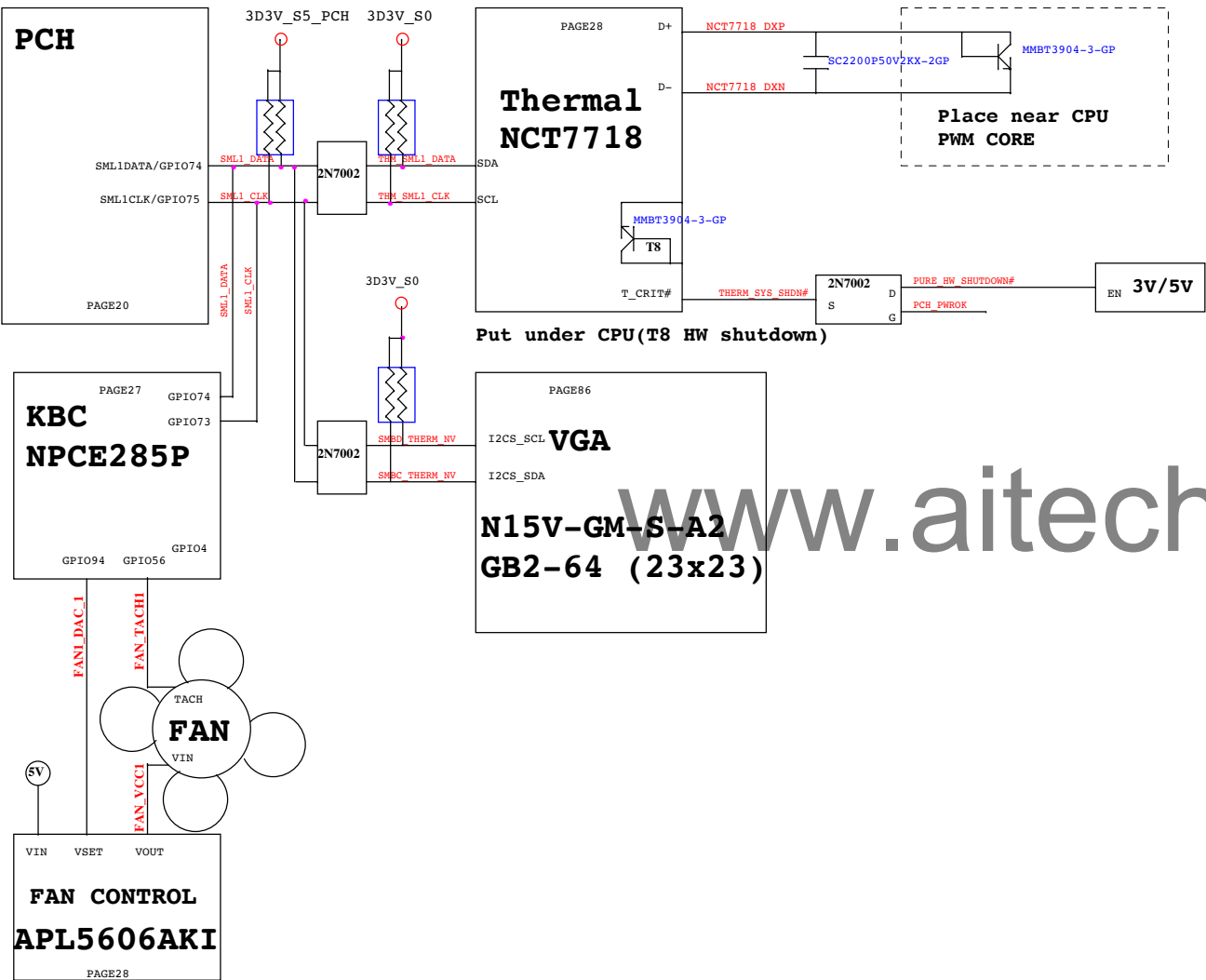
KBC SMBus Block Diagram



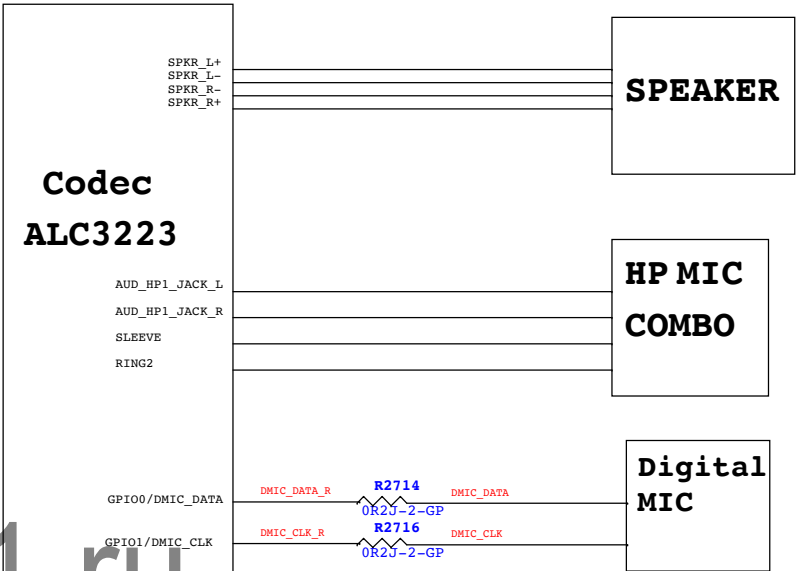
CLK Block Diagram



Thermal Block Diagram



Audio Block Diagram



Change notes -

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